

Study of Crystalline Silicon Solar Cell Fabrication Technology

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ABSTRACT

Study of Crystalline Silicon Solar Cell Fabrication Technology has been presented in this research. This study includes solar cell configurations such as monofacial, bifacial or back contact solar cells. Solar cell efficiency that increased in early phase due to semiconductor processing, contact resistance 16% to 25% in second phase after eighties for wafer quality, minority carrier lifetime. The study also includes manufacturing cost which refers to silicon wafer thickness that represents 50 % cost of a solar panel. Then, the production costs, module costs, system costs. The costs of the solar module are dependent on the number of cells within the module, which is multiplied by the costs of the cells. The wafer thickness has been reduced from 400 μ m to 200 μ m. Thereafter, the fabrication process diagrams for solar cells manufacturing has been presented. Industrial solar cell manufacturing of crystalline silicon solar cells whether it is with a toxic SiH4 and POCl3 based or Saline and POCl3 free fabrication process, they all share the common fabrication steps in the process diagram are wafer inspection, damage removal & texturing and screen printing Ag/Al. Varies in the emitter formation step as POCl3 diffusion, Phosphoric acid diffusion, thermal oxidation or in-situ oxidation. Rapid thermal processing (RTP) is a semiconductor manufacturing process which heats silicon wafers to temperatures exceeding 1,000°C for not more than a few seconds in order to affect its electrical properties. The light current-voltage (LIV) measurements for solar cells have been presented as well. The performance reduction is attributed to reduced passivation, poor minority carrier lifetime and high reflection losses.

How to cite this paper: M. N. Islam | M. S. Alam | M. A. S. Haque "Study of Crystalline Silicon Solar Cell Fabrication Technology" Published in International Journal of Trend in Scientific Research and Development (ijtsrd), ISSN: 2456-6470, Volume-9 | Issue-6, December 2025, pp.772-778, URL: www.ijtsrd.com/papers/ijtsrd99871.pdf



IJTSRD99871

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KEYWORDS: Solar Cells, Configurations, Efficiency, Manufacturing Cost and Fabrication Process Diagrams.

1. INTRODUCTION

Despite the numerous attempts at making better solar cells by using new and exotic materials, the reality is that the photovoltaics market is still dominated by silicon wafer-based solar cells. This means that most solar cell manufacturers are currently equipped to produce this type of solar cells. Consequently, a large body of research is being done all over the world to manufacture silicon wafer-based solar cells at lower cost and to increase the conversion efficiencies without an excessive increase in production cost [1]. In this regard, a detailed, cost-based analysis of advanced solar cell manufacturing technologies aimed at higher (~ 22 %) efficiency with existing equipment and manufacturing processes has been presented. band-gap engineering for enhanced optical absorption, and newer, advanced solar cell configurations including partially transparent bifacial

and back contact solar cells will be required. Highest internal quantum efficiency with least integrated surface reflectance in the visible region and higher reflectance in UV and IR region due to light escaping in the solar cell [2]. In [3], gives an overview of the materials and methods used for fabrication of monocrystalline silicon solar cell using phosphorous diffusion technique. The efficiency of p-n junction solar energy converters, a limiting efficiency, called the detailed balance limit of efficiency, has been calculated for an ideal case in which the only recombination mechanism of electron-hole pairs is radiative as required by the principle of detailed balance. In determining the detailed balance limit of efficiency, the efficiency has been defined in the usual way as the ratio of power delivered to a matched load to the incident solar power impinging

on the cell [4]. The simplified cost model by which the impact of a cell production innovation on the cell cost and the subsequent value-added stages can be calculated. With this approach, one does not need to have a detailed knowledge of the costs of the entire PV production chain, but only be aware of the share of area-proportional costs for each stage of the value chain. The basic idea behind the approach is the comparison of the cost and efficiency impact of a new cell development in contrast to a well-known reference technology [5]. In the current research, study of crystalline silicon solar cell fabrication technology has been presented. This study comprises solar cell configurations, efficiency, manufacturing cost and the fabrication process diagrams for industrial solar cells manufacturing. The light current-voltage (LIV) measurements for solar cells also have been presented.

2. Methodology

Although, there are numerous attempts at making better solar cells by using new and exotic materials, the photovoltaic market is still dominated by silicon wafer-based solar cells.

2.1. Solar Cell Configurations

Fig.1 describes three basic crystalline Si solar cell configurations [6]. These are differentiated from each other by the way sunlight exposure creates electron-hole (EH) pairs. In the monofacial solar cell (Fig.1-a), front surface metallic grid forms one electrical contact with the rear surface fully metallized serving as the second electrode; in bifacial solar cell(Fig.1-b) front and back surface metallic grids are identical. Both surfaces have the capability to generate EH pairs. The bifacial solar cell fabrication process is slightly more involved than the monofacial. In order to achieve high efficiency, these solar cells would require high minority carrier lifetime. In back-contact solar cell configuration (Fig.1-c), both negative and positive electrodes are formed on the rear surface; front surface has no metal grid. Such cells require high minority carrier lifetime since the EH pairs have to diffuse to the back surface for collection and generation of external current. The back-contact solar cell manufacturing process is complicated and requires multiple alignment steps.

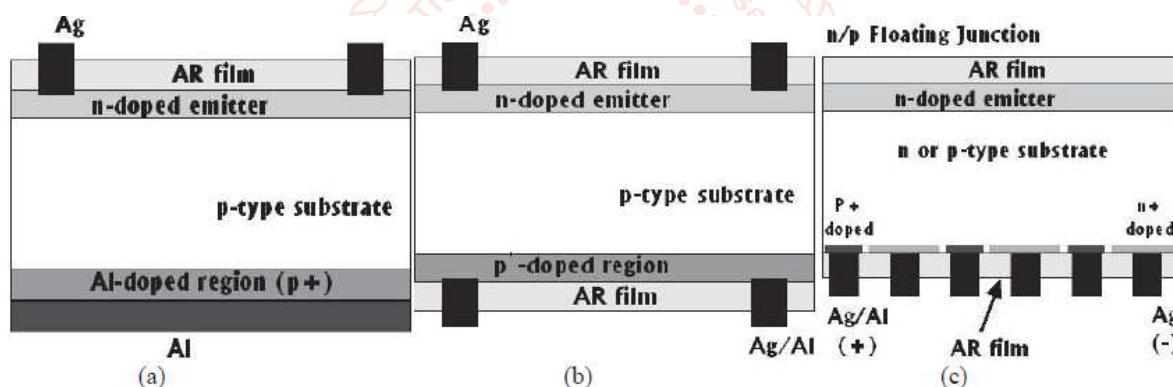


Fig.1: Describes three basic crystalline Si solar cell configurations.

2.2. The Efficiency

The efficiency of p - n junction solar energy converters, a limiting efficiency, called the *detailed balance limit* of efficiency, has been calculated for an ideal case in which the only recombination mechanism of electron-hole pairs is radiative as required by the principle of detailed balance. The efficiency is also calculated for the case in which radiative recombination is only a fixed fraction f_c of the total recombination, the rest being nonradiative. Efficiencies at the matched loads have been calculated with band gap and f_c as parameters, the sun and cell being assumed to be blackbodies with temperatures of 6000^0K and 300^0K , respectively. The maximum efficiency is found to be 30% for an energy gap of 1.1 ev and $f_c= 1$. Actual Junctions do not obey the predicted current-voltage relationship [4]. Solar cell efficiency that increased in early phase due to semiconductor processing, contact resistance 16% to 25% in second phase after eighties for wafer quality, minority carrier lifetime. A third wave of efficiency enhancement, if any, would likely be related to a fundamental change either in manufacturing technology or perhaps bandgap engineering since fundamental limits to solar cell efficiency have likely been reached.

In determining the detailed balance limit of efficiency, the efficiency calculated below is defined in the usual way as the ratio of power delivered to a matched load to the incident solar power impacting on the cell. The following sections present a step-by-step calculation of this efficiency as a function of the essential variables, including several which may reduce the efficiency below the detailed balance limit. Three of these variables have the dimensions of energy and can be expressed as temperatures, voltages or frequencies. These variables are:

the temperature of the sun T_s ,

$$kT_s = qV_s \quad (2.2.1)$$

The temperature of the solar cell T_c ,

$$kT_c = qV_c \quad (2.2.2)$$

and the energy gap E_g ,

$$E_g = h\nu g = qV_g, \quad (2.2.3)$$

where k is Boltzmann's constant, $q = |q|$ is the electronic charge, and h is Planck's constant. The efficiency is found to involve only the two ratios

$$X_g = E_g/kT_s \quad (2.2.4)$$

$$X_c = T_c/T_s \quad (2.2.5)$$

To a very good approximation the efficiency is a function η , "eta" (X_g , X_c , T_s , f) of four variables. T_s = the probability that a photon with $h\nu > E_g$ incident on the surface will produce a hole-electron pair. The value of f for the highest efficiency, corresponding to the detailed balance limit, is determined by the solid angle subtended by the sun [4].

2.3. Manufacturing Cost

c-Si based photovoltaic (PV) price has been reduced by a factor of 250 over last twenty years (from ~ 76 USD to ~ 0.3 USD); its market growth is expected to reach 100 GWP by 2020. Manufacturing cost which refers to silicon wafer thickness that represents 50 % cost of a solar panel. First of all, the costs of the solar module are dependent on the number of cells within the module, which is multiplied with the costs of the cells. Then, the production costs refer to cost of cell production, cell costs. As all concepts can be fabricated on equivalent wafers, the costs of the wafer are simply added to cell production costs, module costs, system costs [5].

2.4. Fabrication Process Diagrams

At SERI, simple, environment-friendly and inexpensive solar cell manufacturing processes have been developed through simplification of typical industrial manufacturing process for p-type wafer solar cells [7].

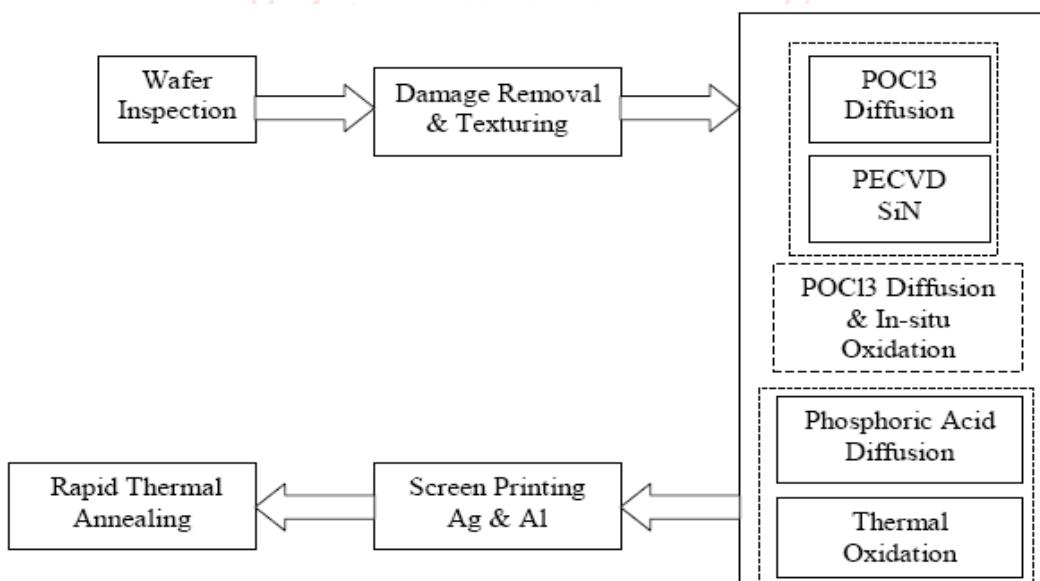


Fig.2: Process diagram for industrial manufacturing of crystalline silicon solar cells.

2.4.1. Wafer Inspection

All incoming wafer properties sheet resistance, lifetime prior to processing are measured since efficiency of the solar cell is ultimately limited by its physical properties. For the structuring processes of the high efficiency solar cell surface it needs p-type, <100> to <156> mono/multi-crystalline silicon wafers, thickness 200-380 μm and 1-2 ohm-cm resistivity [8].

2.4.2. Damage Removal & Texturing

Solar cell fabrication requires cleaning and texturing of wafers. Cleaning is done for the removal of the organic contaminants, thin oxide layer and metal particles and texturing is done to create random, sub-wavelength

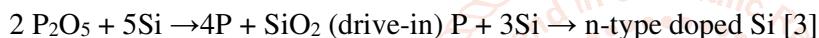
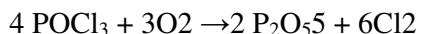
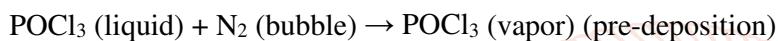
pyramid features on wafer surface to reduce reflection and enhance light absorption [9-10]. This kind of processing requires wet-chemical processing benches, exhaust system and water treatment prior to discharge to the waste stream. Cleaning and texturing of wafer is done by three processes are saw damage removal process, hydrophobic process and texturing process [3].

2.4.3. Emitter Formation

In almost all industrial manufacturing, the emitter formation is accomplished using liquid source POCl_3 diffusion and plasma-enhanced chemical vapor deposition (PECVD) SiN ; POCl_3 Diffusion & In-situ Oxidation and Phosphoric Acid Diffusion & Thermal Oxidation.

2.4.3.1.1. POCl_3 Diffusion

Phosphorus oxychloride (POCl_3) is a liquid source which vaporizes at room temperature itself hence it should be kept in cool place. Generally, phosphorous diffusion process is performed in two steps. The first step is called pre-deposition that involves the formation of phosphorous-rich oxide films on the silicon substrate. Second step is called drive-in [11-12] where the phosphorous-rich oxide film acts as an infinite source for phosphorous diffusion into the Si substrate. During pre-deposition, phosphorus pentoxide (P_2O_5) forms on the surface of the wafers by the reaction of phosphorous with oxygen. The P_2O_5 immediately reacts with the silicon, by resulting in diffusion of phosphorus and formation of the phosphosilicate glass (PSG) $[\text{SiO}_2: (\text{P}_2\text{O}_5)_x]$ layer on the Si surface. The phosphorus atoms formed at the PSG-Si interface penetrate through the silicon wafer [13] and can be simplified with the following reaction equations:



2.4.3.1.2. PECVD SiN

Surface passivation and reflection reduction is achieved with plasma-enhanced chemical vapor deposition (PECVD) of SiN using NH_3 (ammonia) and SiH_4 (silane) gases. Both of these gases have toxic effects and are harmful to the environment. In addition, PECVD is often times the most expensive processing step in terms of equipment, its maintenance and processing of exhaust gases.

2.4.3.2. POCl_3 Diffusion & In-situ Oxidation

In the new process, PECVD SiN step has been replaced by an oxide film grown in-situ during the POCl_3 diffusion process. An oxidation step is added to the conventional POCl_3 diffusion process, the thickness of the oxide is controlled to achieve blue surface reflectance. Annealing process parameters were optimized to achieve tunneling through the oxide layers. This new process reduces costs and leads to environment-friendly manufacturing through elimination of toxic gases and excessive chemical usage; it also eliminates the most expensive equipment in the manufacturing line. The new process does not require any modification of existing manufacturing equipment and processes. Solar cells fabricated with the silane-less process have lower efficiency than the 18 % industrial solar cell with SiN passivation.

2.4.3.3. Phosphoric Acid Diffusion & Thermal Oxidation

The industrial solar cell manufacturing uses toxic POCl_3 chemical in emitter formation step. A nontoxic, solar cell fabrication process has been developed by replacing POCl_3 chemical with phosphoric acid [14]. There are several advantages of this approach: elimination of toxic POCl_3 chemical, in-house synthesis of phosphoric acid diffusion solution, and lower cost. Fabrication process sequence for this POCl_3 -less, Silane-less, oxide-passivated solar cell has been drawn in Fig.2 in contrast with the silane-less solar cell processing. The POCl_3 diffusion and in-situ oxidation steps have been replaced by two steps: phosphoric acid diffusion and thermal oxidation. Solar cells fabricated with this new process have exhibited efficiencies similar to that of silane-less solar cells.

2.4.4. Screen Printing Ag & Al

Screen printing process is most commonly used to form metal contacts on back and front surfaces of solar cells. Following diffusion, screen printed metallic contacts are formed to form electrical contacts to n and p doped regions. A thick, viscous metal solution or paste is forced through stainless screen grid onto the wafer in selected lithographically defined open regions in the screen. The metal lines on the front surface (n-type) are made of silver and on the back surface (p-type) are made of aluminum. Aluminum contact on the wafer backside also serves to form a heavily diffused p++ layer that reduces contact resistance and enhances back surface

reflectance. Appropriately-designed screens are used for this process, and screen printers are used to form Ag and Al contacts in front and back surfaces of the solar cell. This process must be tightly controlled for temperature, pressure, speed, and many other variables. After each printing step the wafer goes to a drying furnace to solidify the paste. The wafer is then transferred to another printer for printing additional lines on either the front or back side of the wafer. Each solar cell has conductive lines on both front and back sides that are printed using screen masks and which have different functions.

2.4.5. Rapid Thermal Annealing

Rapid thermal Annealing (RTA) in rapid thermal processing is a process used in semiconductor device fabrication which involves heating a single wafer at a time in order to affect its electrical properties. Rapid thermal processing (RTP) is a semiconductor manufacturing process which heats silicon wafers to temperatures exceeding 1,000°C for not more than a few seconds. During cooling water temperatures must be brought down slowly to prevent dislocations and wafer breakage due to thermal shock. Unique heat treatments are designed for different effects. Wafers can be heated in order to activate dopants, change film-to-film or film-to-wafer substrate interfaces, densify deposited films, change states of grown films, repair damage from ion implantation, move dopants or drive dopants from one film into another or from a film into the wafer substrate[15].

2.4.6. LIV Measurements

In order to measure solar cell performance, the positive and negative probes are connected to an electronically-controlled resistive system. As the resistance in the electronics load unit increases, the current flow is reduced as determined by Ohm's law. At high enough resistance values, no current can flow through an external circuit. At this point solar cell exhibits the highest voltage which is known as the cell open-circuit voltage (V_{OC}) as shown in fig.3. Solar cell maximum current is achieved as the resistance is reduced to a minimal value. This corresponds to cell short-circuit current (I_{SC}). As a function of resistance, solar cell I-V curve traces the path determined by the box-like curve described in fig.3. Maximum power is achieved at the maximum power point (MPP) at which the product $P=V*I=V_m*I_m$ is at its maximum value. The ratio of V_m*I_m to $V_{OC}*I_{SC}$ is called solar cell/panel fill factor (FF).

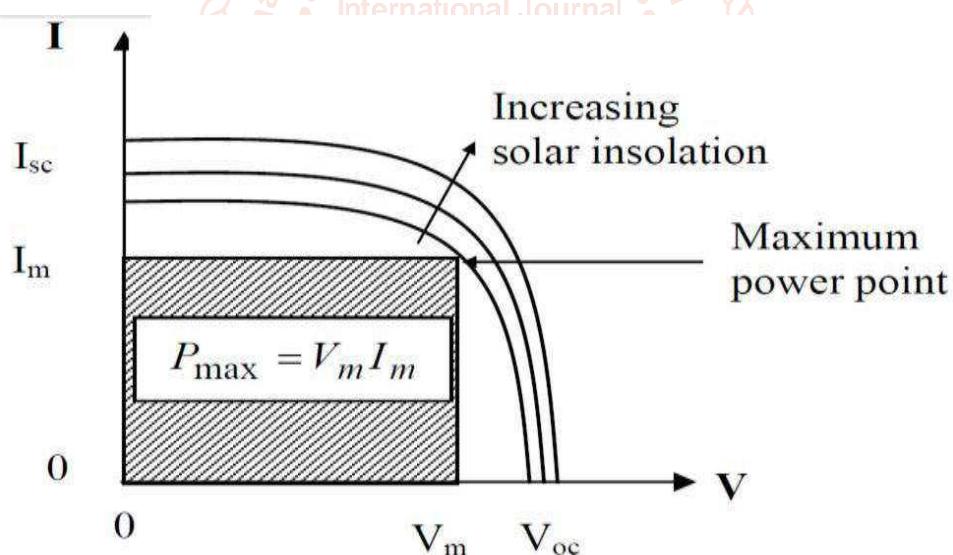


Fig.3: Typical solar cell LIV measurements as a function of increasing sunlight.

$$\text{Solar Panel, Fill Factor (FF)} = V_m * I_m / V_{OC} * I_{SC}$$

FF is a complicated function of many variables including resistance, minority carrier lifetime, surface recombination. it usually in the range of 0.6-0.8, The higher FF represents the higher efficiency of the solar cell [16].

A solar cell's energy conversion efficiency (η , "eta") is the percentage of power converted (from absorbed light to electrical energy) and collected, when a solar cell is connected to an electrical circuit. This term is calculated using the ratio of P_m , divided by the input

light irradiance under "standard" test conditions (E , in W/m^2) and the surface area of the solar cell (A_c in m^2) [17].

$$\eta = \frac{P_m}{E \times A_c} \quad (2.4.6.1)$$

3. Discussion

Demand for renewable energy continually increases due to environmental pollution and resource depletion caused by the increased use of fossil fuels. Among the various renewable energies, the solar cell developed by numerous researchers has been widely used

because of its advantages, ease of use and low maintenance cost. Although, there are numerous attempts at making better solar cells by using new and exotic materials, the photovoltaic market is still dominated by silicon wafer-based solar cells. Currently, 95% of all industrial solar cells are fabricated from p-type substrates and the industry technology roadmap for photovoltaics (ITRPV) predicts that this dominance will continue with over 65% by 2026. In this context, study of crystalline silicon solar cell fabrication technology has been presented in this research. Industrial solar cell manufacturing/fabrication of crystalline silicon solar cells from p-type silicon wafer requires the emitter formation step whether it is with a toxic SiH₄ and POCl₃ based or Saline and POCl₃ free, Phosphoric acid diffusion, thermal oxidation or in-situ oxidation followed by wafer inspection, damage removal & texturing in pyramids structure. Then the screen printing with Ag/Al formation of electrical contacts (anode/cathode). Thereafter, the rapid thermal processing (RTP), semiconductor manufacturing process, heats silicon wafers to temperatures exceeding 1,000°C for not more than a few seconds in order to affect its electrical properties. At the end, the light current-voltage (LIV) measurements for electrical performance determination of solar cells as shown in Fig.3. The performance reduction is attributed to reduced passivation, poor minority carrier lifetime and high reflection losses.

The manufacturing cost which refers to silicon wafer thickness that represents 50 % cost of a solar panel. The wafer thickness has been reduced from 400 μ m to 200 μ m. Then, the production costs, module costs, system costs. The costs of the solar module are dependent on the number of cells within the module which is multiplied by the costs of the cells. Solar cell efficiency that increased in early phase due to semiconductor processing, contact resistance 16% to 25% in second phase after eighties for wafer quality, minority carrier lifetime. The third wave of efficiency enhancement, if any, would likely be related to a fundamental change either in manufacturing technology or perhaps bandgap engineering since fundamental limits to solar cell efficiency have likely been reached. The solar cell configurations are monofacial, bifacial or back contact solar cells as shown in Fig.1. The key features of the three solar cell manufacturing approaches and the fabrication process diagrams for industrial solar cells manufacturing are shown in Fig.2. Surface texturing processes are changed from microscale to nanoscale for the reduction of reflection; although the textures have not yet been fully optimized. SiN anti-reflection and passivation films have been successfully replaced

by oxide passivation and finally, toxic POCl₃ chemical has been replaced by much more benign phosphoric acid. It is worth noting that phosphoric acid is often used in foods and soft drinks.

4. Conclusion

Study of crystalline silicon solar cell fabrication technology has been presented in this research. This study comprises solar cell configurations monofacial, bifacial or back contact solar cells, efficiency usually 16% to 25% which depends on semiconductor processing, contact resistance, wafer quality, minority carrier lifetime, fundamental change either in manufacturing technology or perhaps bandgap engineering. The manufacturing cost and the fabrication process diagrams for industrial solar cells manufacturing also have been presented. The steps in the process diagram are wafer inspection, damage removal & texturing, the emitter formation and screen printing Ag/Al, rapid thermal processing (RTP) and the light current-voltage (LIV) measurements in almost all industrial solar cells manufacturing. Although, there are numerous attempts at making better solar cells by using new and exotic materials, the photovoltaic market is still dominated by silicon wafer-based solar cells.

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