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Toward Dependable AI/ML Hardware: Reliability Strategies Across Architectures and Memory Systems: Survey Paper

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ABSTRACT

AI/ML workloads are becoming more widely used while their reliable hardware execution stands as a crucial factor especially when considering aggressive technology advancements and NVM technology adoption. The special session demonstrates extensive research into reliability enhancement methods for AI/ML hardware infrastructure at architectural and system-levels and design-time through neuromorphic and multiprocessor system studies. The discussion highlights three chief technical points which include elevated fault sensitivity of systems and aging mechanics due to voltage effects as well as the sustaining of reliability against hardware decay. The research shows breakthrough approaches which comprise Rox-ANN for efficient ANN implementation and PALP and DATACON methods for PCM memory optimization as well as MNEME and HEBE systems to manage NVM and hybrid memory aging and RENEU for neuromorphic reliability modelling under workload conditions. This work studies system-level methods that integrate thermal-aware task mapping and aging-aware checkpoint distribution and performs a combined analysis between DVFS and replication techniques in multiprocessor task scheduling. These solutions achieve substantial advancements regarding system energy efficiency coupled with increased performance while lengthening the system operational period. Experimental tests performed on SPEC CPU2017 and MiBench as well as diverse ML operations demonstrate the need for implementing early-stage reliability modelling approaches with workload management techniques that understand applications and architecture specifications to develop dependable AI/ML hardware systems.

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INTRODUCTION

The recognition and classification operations benefit largely from Artificial Neural Networks (ANNs). Embedded systems need pre-trained Artificial Neural Networks to operate with low-precision fixed-point formats though data and network parameter conversion demands possible retraining procedures. The multiply-accumulate operation stands as a major limiting factor when it comes to high resource and energy usage in such implementations. Rox-ANN represents a new design strategy for implementing ANNs through processing elements optimized for FPGA implementation. The processing elements apply reduced precision fixed-point numbers in combination with fast yet power-efficient approximate multiplier technologies. The implementation method begins with trained network parameter analysis and clusterization for reducing approximate multipliers' quantity. Rox-ANN offers fast hardware implementation capabilities which produce results within expected tolerances. Our methodology obtained validation through testing a MNIST digit recognition task using a LeNet-based ANN. The evaluation shows 65.6% area reduction combined with 55.1% energy savings and 18.9% latency decrease through the use of 8-bit precision and approximate arithmetic units as compared to conventional 16-bit precision and accurate arithmetic units. [1]. A white paper in this chapter describes how to design a platform which extends neuromorphic systems towards reaching brain-scale complexity. The proposed system exists for large-scale search operations during biological data interface activities.

The design works to match both nerve cell counts and synaptic pathways that appear in an adult human brain. The major obstacle in achieving this goal stems from the huge complexity that emerges by linking trillions of neurons through synapses. A practical architectural design is introduced in this chapter to regulate the huge bandwidth requirements needed for operating large-scale neuromorphic systems. Neuromorphic computing achieves its full potential by making computational capabilities available like the human brain along with its energy-efficient dimensions. The chapter develops a new inter-cluster communication network based on current system-on-chip (SoC) design progress. The network operates as an effective approach to manage worldwide synaptic communications while it connects distinct arrays of synapses within local clusters. The core architecture contains a power-efficient switching operation located in the CMOS back end of line (BEOL). A point-to-point communication network provides dedicated dynamic connections between clusters which outdoes traditional bus-based networking by enhancing both efficiency and flexibility of communication. [2]

Li-passivation in zigzag GaN nanoribbons significantly modifies their electronic properties, enhancing Fermi velocity and reducing effective mass to improve carrier mobility. DFT investigations further show strong gas adsorption and charge transfer, highlighting their potential as high-performance nanosensors[3-4]. A design-technology analysis occurs in this paper for building a fully connected neural network utilizing non-volatile OxRRAM cells. The substantial need for numerous distinct weight levels at synapses creates an essential obstacle for implementing all synapses using a single non-volatile memory device. The proposed "mixed-radix coding method" applies multi-device synaptic elements to deliver 94% classification precision although it operates with device-level non-uniformities. This research stands as the initial study that examines the design and technological trade-offs between single-device and multi-device synapses through experimental silicon characterization. Our research unveils that the neuromorphic algorithm proves resistant to substantial variations. The experimental data was obtained from a 1Mb OxRRAM array within the research[5-6].

NVM-based dense crossbar arrays represent an effective method through which massively parallel neuromorphic computing systems can be achieved with energy-efficiency in mind. This research starts with an analysis of how NVM devices have been applied to create new implementation systems for three main computational frameworks including spiking neural networks (SNNs), deep neural networks (DNNs), and "Memcomputing". The local learning rules including spike-timing-dependent plasticity (STDP) can modify NVM-based synaptic connections for implementing biologically inspired changes within SNNs. NVM arrays function as an experimental form of synaptic weight matrices to enable backpropagation training along with essential matrix–vector multiplications through parallel execution with reduced energy consumption. The proposed analog computing system demonstrates better power efficiency combined with higher speed than GPU algorithms particularly when implementing industrial-level applications. Our paper investigates current research on different NVM systems which utilize phase-change memory (PCM) together with conductive-bridging RAM (CBRAM) and filamentary and non-filamentary RRAM along with various next-generation NVMs in their application as neuronal components and synaptic units within neuromorphic systems. Technological evaluation depends on five main properties including conductance dynamic range, linearity and symmetry of conductance response, retention time, endurance cycles and switching power demands as well as device variability tolerance. [7]

PCM devices utilize multiple banks for parallel memory requests because they store data in separate partitions. Each bank requires independent but shared peripheral structures for sense amplifiers and write drivers. System performance decreases when multiple requests focus on the same bank because requests must execute one by one. A contemporary PCM bank consists of multiple partitions which function autonomously through central peripheral components with major ones being sense amplifiers for read functions and write drivers for write functions. We have developed "PALP" (Partition-Level Parallelism) as a novel approach to achieve internal parallel processing at the partition level within the bank. Through PALP the scheduling logic of the memory controller enables exploitation of concurrency between partitions. PALP makes three key contributions. PALP implements new PCM commands which allow simultaneous partition access to single banks through its conflict-mitigating approach that modifies nothing in PCM interfaces or internal structure. A new operating mode exists in the proposed modest circuit enhancements to the write drivers. The write drivers operate under this new mode to help sense amplifiers solve read-read conflicts which leads to better concurrency. We have created an access scheduling mechanism which gives preference to memory requests that benefit from

partition-level parallelism operations but maintains both starvation-free operations and satisfies PCM power consumption constraints. The evaluation of PALP relies on benchmarks from both MiBench and SPEC CPU2017 suites. PALP delivers 28% better system performance and realizes 23% reduced PCM access latency which surpasses the current state-of-the-art technical solutions. [8]. DFT-based studies demonstrate that Indium Nitride nanoribbons can effectively detect gases like CO, CO_2, NO, and NO_2 due to notable charge transfer and band structure modulation. Similarly, Scandium Nitride monolayers show strong adsorption sensitivity toward toxic gases such as NH_3, AsH_3, BF_3, and Bcl_3. Zigzag silicon carbide nanoribbons exhibit enhanced gas sensing performance through improved electronic response to hazardous gas molecules, making them promising for advanced sensor applications[9-11].

The rise of computing systems resorts to hybrid memory architectures that blend DRAM with non-volatile memory (NVM) for realizing both swift operations and solid reliability and compact footprint. Hybrid memory systems face the major obstacle of inter-memory asymmetry which causes NVM latency to exceed that of DRAM. Parasitic elements extending along bitlines produce highly significant delays that affect both DRAM and NVM operations while simultaneously increasing voltage requirements thus reducing NVM reliability. A "tiered memory architecture" divides each long bitline in DRAM and NVM through an isolation transistor into dual segments. Low-voltage accelerated access along with short latency characterizes the memory segments positioned next to sense amplifiers which leads to "intra-memory asymmetry" inside each storage type. This modified design method allows DRAM-NVM hybrid systems to make performance-related reliability choices. The comprehensive platform solution "MNEME" enables operating system memory management to leverage both kinds of memory asymmetry. With its innovative approach MNEME basically improves current page migration methods through three important mechanisms. The system allows optimally placing and moving individual pages between different memory tiers within DRAM and NVM. Page allocation becomes more efficient because the system effectively predicts data access rates to place content at proper levels thus reducing the need for resource-intensive migration operations while running programs. The mechanism works with low overhead to move pages between tiers of equivalent memory type without using up memory channel bandwidth. MNEME demonstrates significant enhancement in both performance and reliability during single-core and multi-programmed workload scenarios because it effectively places data within hybrid tiered memory systems. The research promotes the essential role of combined architectural-level OS co-design for overcoming memory asymmetries so hybrid memory systems operate at their best. [12]. The memory technology called "Phase-change memory (PCM)" integrates features of DRAM speed with Flash capacity in one non-volatile solution. PCM's writing operations come with elevated time delays and power requirements which exceed reading operations. The write energy and latency of memory cells show high dependency on two factors which include the input data as well as the stored content at the corresponding location. The programming method for memory locations that contain all-zeros or all-ones data requires only SET or RESET operations and delivers more efficient writing than programming unknown data because it does not need bidirectional writing capability.

The paper presents DATACON as a data content-aware PCM write mechanism designed to bring down write energy expenses and latency through selective redirection of write commands to memory cells containing established content (all-zeros or all-ones). DATACON operates in three phases. DATACON uses overwriting of unknown content exclusively during unavoidable situations. The system performance improvement reaches 27% while providing 31% faster write access latency and down to 43% lower memory energy requirements according to evaluations from DATACON across the studied benchmarks including SPEC CPU2017, NAS Parallel Benchmarks, and modern machine learning workloads. [13]. Computing systems today choose non-volatile memory (NVM) because it enables the construction of both powerful and inexpensive main memory. NVM operates at higher voltages that cause CMOS transistors in memory bank peripheral circuitry to age more rapidly. Device scaling along with increasing power density results in higher operating temperatures that worsens aging effects and reduces the reliability and extends the longevity of NVM-based systems. We introduce "HEBE" which represents an architectural solution to reduce NVM-based main memory peripheral circuit aging. The main elements of HEBE include three distinct innovations. The SPEC CPU2017 benchmarks reveal our system HEBE achieves substantial NVM lifetime extension while simultaneously enhancing the entire system performance along with operational efficiency[14].

The Phase-Change Memory technology demonstrates powerful characteristics as an NVM solution because it delivers storage-class memory characteristics with

DRAM-like access latency and SSD-grade storage density. PCM demonstrates two advantages that support its application in neuromorphic computing since it utilizes MLC structures to deliver efficient synaptic storage in elaborate brain-wired frameworks. The broad-market adoption of PCM systems encounters two major hurdles which prevent their increased use. The process of writing data to PCM cells requires more energy while taking longer execution time leading to reduced system performance and power inefficiency. Device reliability problems arise from the need to use high operating voltages required for programming cells because these voltages increase the rate of device degradation. The authors identify core challenges in this work then implement architectural and system-level solution methods to reduce them. Our approach matches "write operation efficiency and controls voltage fluctuations while boosting system execution and power savings and device trustworthiness." These strategies aim to enhance sustainability through lifetime extension of PCM devices while minimizing the memory-intensive application energy usage. Our research helps enable practical use of PCM technology for main memory hierarchies together with neuromorphic systems as it solves performance versus reliability trade-offs found in PCM technology which advances the development of efficient and scalable computing systems. [15]

Machine learning workloads run with energy efficiency when neuromorphic hardware uses non-volatile memory as its NVM technology. PCM and other NVM technologies need high operating voltages which charge pumps on-chip must generate. Non-stop operation of these charge pumps triggers "internal stress accumulation" within CMOS parts which speeds up "degradation from negative bias temperature instability (NBTI)" until reliability declines. The practice of forcefully draining the charge pump reduces aging but causes the temporary suspension of neuromorphic hardware that adversely affects both system performance and workload precision and delay times. The proposed workload-aware framework creates a balance between performance rates and reliability aspects in neuromorphic systems. The proposed framework divides its operation into two distinct stages. The first stage of the framework determines how long the charge pump needs to activate while performing specific workloads. Additional data from a characterized NBTI aging model together with activation time information determines estimations about charge pump degradation when operating under different conditions. The framework analyses how different SNN mapping methods together with charge pump power-distribution techniques affect both neuromorphic system performance and reliability levels the analysis enables system designers to utilize this framework for design-time trade-off exploration which enables them to make more knowledgeable reliability-oriented design margin decisions. The proposed approach guides the development of sustainable reliable neuromorphic computational systems which best serve strict requirements for performance and longevity. [16]

Neuromorphic hardware reliability suffers from "critical ageing problems" due to "NBTI and TDDB" because "non-volatile memory (NVM)" requires high voltage and current access in scaled process technologies. The mechanisms used to access NVM synapses result in high voltage demands and strong current requirements thus causing rapid deterioration of peripheral CMOS circuits. Standard reliability tests impose excessive restrictions by assuming maximum operational parameters which lead to an incorrect restriction of hardware performance capabilities. This paper introduces RENEU as a reliability-oriented framework which enables machine learning workload allocation to neuromorphic hardware systems. The RENEU framework strives to boost complete system reliability levels through mechanisms that do not produce noteworthy delays in execution. The RENEU system brings a "unique aging model" which analyses various hardware failure effects that affect CMOS circuits operating in neuromorphic systems. Through its model RENEU produces an expansive trade-off region between reliability and performance where design space exploration occurs with Particle Swarm Optimization (PSO). The algorithm uses Pareto optimization to establish optimal connections between neurons and synapses which yield suitable mergers of system durability and operational functionality. The evaluation of RENEU operates across different machine learning applications which utilize state-of-the-art neuromorphic hardware based on NVM synapses. The experimental data reveals that RENEU achieves circuit aging reduction of 38% in standard operation which results in 18% longer hardware operational time but demands only 5% extra performance consumption than optimized baseline implementations. RENEU creates sustainability opportunities for neuromorphic hardware systems that last longer because it systematically integrates reliability requirements throughout the application mapping process. [17]

The neurobiological system of neuromorphic computing with NVM provides an efficient hardware solution to run machine learning operations through spike-based bio-inspired computations and learning

methods. PCM-based NVM technologies demand high operating voltages that expedite both peripheral CMOS neuron circuit aging and reduce neuromorphic hardware longevity. We assess the sustained reliability effects of present-day machine learning applications executing on neuromorphic systems through implementation of authentic failure models which combine negative bias temperature instability (NBTI) and time-dependent dielectric breakdown (TDDB). The aging mechanisms intensify due to the high-voltage operation frequency required when accessing synaptic weight cells based on NVM technology. Our research investigates the development of a technology which combines "reliability analysis into neuromorphic processing techniques". We evaluate the reliability-performance relationship of neuromorphic circuit stop-and-go execution using a periodic relaxation method which enables device resting to decelerate aging and increase device lifespan. The neuromorphic system displays significant capability to reduce aging impacts when relaxation phases are positioned strategically within workload execution while sustaining low operational impact. The paper demonstrates the critical need to integrate "reliability modelling and workload management tools" at the beginning of neuromorphic system design to support "long-duration operational sustainability". [18]

The combination of power density and temperature variations becomes a critical reliability factor in multiprocessor systems since it speeds up device wear-out events and results in permanent faults. Our proposed approach functions as a performance-aware system-level application mapping solution which optimizes energy efficiency as well as temperature-induced aging during multimedia workload execution on multiprocessor systems. Our method includes a basic thermal model that effectively represents both short and long-term temperature patterns and core-to-core temperature relationship. The validation results show that this model achieves temperature forecasting accuracy rate of "5.5°C" while maintaining an estimation of "MTTF that matches state-of-the-art techniques to a 21% extent" when tested against the leading "Hot-Spot simulator". This fast gradient-based heuristic uses core voltage and frequency control to reduce temperatures and achieve longer system duration along with decreased total energy usage. Task remapping operates within modern multiprocessors as a supported capability through the reliability model. The proposed linear programming formulation allows efficient core management among multiple active tasks to achieve optimal lifetime duration. Our technique achieves modifications to synchronous data flow graphs by producing a 47% enhancement in hardware lifetime or a 24% decrease in energy consumption as witnessed during experimental phases. The core distribution system we designed specifically for concurrent applications raises average system lifespan by 10% when compared to standard core allocation based on performance goals. [19].

Density Functional Theory (DFT) investigations reveal that Cu and Fe doping in boron nitride nanoribbons (BNNRs) significantly enhances their electrical conductivity, making them suitable candidates for nanoscale interconnects in advanced integrated circuits. Ab-initio studies on aluminum nitride nanoribbons (AlNNRs) demonstrate their potential in implementing reconfigurable logic gates due to tunable electronic properties under external stimuli. Additionally, the design of a FinFET-based operational amplifier (Op-Amp) using 22 nm high-k dielectric technology shows promising results in reducing leakage currents and enhancing performance, offering a robust solution for low-power, high-efficiency analog circuit applications[20-21].

Modern applications need diverse computing demands so "Reconfigurable Multiprocessor Systems (RMPSoCs)" combine homogeneous multiprocessor systems and a reconfigurable area to gain popularity. Price-specific task mapping occurs on these platforms because developers separate programs into GPP-executed software tasks along with hardware tasks that run in the reconfigurable area. The design requirements of performance reliability and cost must be met by task mapping procedures. The main difficulty in this context involves achieving an optimal balance between short-term fault resilience against permanent system reliability. The intensification of checkpoint numbers improves soft error resilience but simultaneously boosts GPP usage and power expenditure which then hastens the aging-induced permanent faults. Previous studies on task mapping and scheduling mostly neglected the reliability trade-off which exists between these operations. A reliability-aware optimization technique serves to determine the best checkpoint number for software tasks. The proposed method extends GPP lifetime by minimizing aging effects and simultaneously delivers maximum transient fault protection to both GPPs and reconfigurable hardware units. The process maintains commitment to both design performance and cost specifications. Our evaluation of the method consists of diverse testing involving synthetic along with real-life application task graphs which contain cyclic and acyclic structures. Our method delivers average platform lifetime expansion of 60% against other existing

techniques for transient fault management. Our gradient-based heuristic enables design space exploration time reduction by up to 500 times without compromising solution quality relative to the optimal results by 5 percent. [22]

The design of present-day Multiprocessor Systems-on-Chip (MPSoCs) requires achieving two paramount goals which are energy efficiency and reliable operation. "Task mapping" stands out as an affordable solution to achieve efficient optimization of energy efficiency and reliability through its task-core assignment process. A multi-objective framework designed to explore design spaces finds the best task-to-core assignment method and frequency and voltage settings for each task so designers can achieve reliability targets within specified energy and performance limits. This work provides a novel reliability model that integrates core aging from extended high voltage and frequency operations as well as transient fault effects because they relate to voltage and frequency. Studies normally examine either isolated elements or parts in their research. The approach establishes "selective task replication" as a mechanism for implementing "soft-error tolerance". The approach combines proactive strategies which consider aging factors in mapping with reactive fault tolerance methods that use replication-based protection. The proposed framework defines energy efficiency and reliability as multiple optimization targets. A genetic algorithm explores the wide design space through the optimization features of task mapping and DVFS combined with selective replication. The method shows its capability through experiments which employ real-life and synthetic application task graphs. Experimental results reveal superior performance for this method compared to contemporary approaches by maintaining an optimal balance between all three metrics of performance levels together with system reliability and power usage which indicates potential success in future MPSoC technology development. [23]

Conclusion

Nowadays reliability stands as a primary consideration in AI/ML hardware because it determines the practical implementation and extended operational lifetime of such systems. The presentation shows that managing upcoming reliability issues in neuromorphic and multiprocessor platforms based on NVM requires an integrated solution which covers fault modeling at the device level and system-level task mapping. The combination of PALP, DATACON, HEBE and RENEU demonstrates how engineering hardware system improvements with task scheduling intelligence can slow down hardware decay processes without degrading performance. Design-time tools need to integrate reliability metrics which include aging-aware models and multi-objective optimization tools to help designers find suitable balances between energy consumption and dependability and performance. The integration of reliability elements during the design stage serves as the fundamental key to build sustainable AI/ML hardware systems.

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