International Journal of Trend in Scientific Research and Development (IJTSRD)
Volume 6 Issue 4, May-June 2022 Available Online: www.ijtsrd.com e-ISSN: 2456 – 6470

A Low Power Solution to Clock Domain Crossing

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ABSTRACT

Because of the increased complexity of designs in recent years, we now have multiple components on a single chip that employ independent clocks, meaning that these clocks are not synchronized. As a result, problems with Clock Domain Crossing will occur, which, if not resolved, will proliferate and destroy the entire chip. Data crossing clock domains can cause a variety of problems, including as metastability and data loss, which can lead to the device failing completely. To overcome the clock domain crossing concerns, this work presents a dual flip flop synchronizer that employs TSPC logic and is based on the SOI technology. TSPC synchronizer when implemented in SOI technology gives outstanding results. It improves the rise time by 46.15 %, the fall time by 28.57 %, dissipates 24.23% less power, power delay product by a huge margin of 59.20 % when compared to its bulk CMOS counterpart. When implemented on a chip, it also takes up the least amount of space. All the circuits are designed in DSCH and simulated in Microwind software.

KEYWORDS: *TSPC, CDC, SOI, Synchronizer, Low Power*

How to cite this paper: Dhatrish Tewari | Mamta Khosla "A Low Power Solution to Clock Domain Crossing" Published in International Journal of Trend in Scientific Research and Development (ijtsrd), ISSN: 2456-6470, Volume-6 | Issue-4, June 2022, pp.1022-1025, URL: www.ijtsrd.com/papers/ijtsrd50222.pdf

IJTSRD50222

1. INTRODUCTION

In order to meet the requirements of high performance and low power, the number of clocks increases with the complexity of the System-on-Chips (SOC) with each successive generation. The clocks in modern SoC architectures are frequently unrelated. Clock Domain Crossing (CDC) difficulties occur when data/signals traverse such unrelated or asynchronous clock domains, leading the system to fail. Such CDC signals must be synchronized between domains using an appropriate synchronizer and validated in some way before quality sign-off.

The global trend towards adopting new technologies increases the demand for electronic devices. The main challenge is to design the most compact device with a low power consumption. As increasingly sophisticated designs are produced, multiple independent clock domains are frequent in complex designs like SoCs, resulting in a large number of CDC crossing paths in the design, where data can suffer CDC challenges such as metastability, data loss, data incoherency, and so on. This problem is likely to worsen, necessitating the development of a synchronizer that can tackle Clock Domain Crossing concerns while using less power, less area and having less delay. This leads us to the stage where we must search for the various logic styles required to create a circuit. We must also move our focus away from traditional Complementary Metal Oxide Semiconductor (CMOS) technology and toward new technologies. Moore's Law continues to stay true, however doubling the number of transistors driving processing power is far more expensive and technically challenging. As we continue to miniaturize computers, we'll almost likely come against Heisenberg's uncertainty principle, which limits precision at the quantum level and so limits our computational capabilities. So, cramming an increasing number of transistors onto a processor solely to boost output isn't going to cut it in the future. As a result, rather than focusing on the traditional CMOS technology, on which we have already expended a great deal of work, we should instead concentrate on some alternative technologies that are now available. Silicon On Insulator (SOI) technology is one such technology, its application in digital circuits has resulted in lower power dissipation and lower delay when compared to traditional CMOS technology.

When compared to other circuit design strategies for synchronizer design, the True Single-Phase clock TSPC methodology has the shortest delay and uses the least amount of power. It also requires fewer transistors, which means that when implemented on a chip, it will take up less space. Also, it uses a True Single-Phase clock thereby not requiring the use of the complement of the clock in the synchronizing circuit, this usage of Single-Phase Clock eliminates the clock overlap race condition. TSPC offers an additional advantage: the possibility of embedding logic functionality into the latches. This reduces the delay overhead associated with the latches. The EV4 DEC Alpha microprocessor and many other high-performance processors adopted this strategy of integrating circuitry inside latches extensively [1].

All these advantages of TSPC and SOI when combined in a single circuit have given the best results of all the compared designs.

2. DESIGN ANALYSIS

There are different digital circuit designing techniques which we can employ to design our circuits. One should use a strategy that serves the circuit's function while also being minimal in power, area, and delay. In this paper, Dual flip flop technique is used to create a synchronizer that will solve the CDC problem. The synchronizer in Figure 1 is made up of 18 transistors and is constructed using the TSPC approach. It's made by joining two back-to-back positive edge triggered flip flops together. When compared to other circuit design strategies, it employs the fewest transistors. So, when compared to alternative circuit design strategies, the synchronizer will take up the least amount of space on the chip, as well as having the least latency and power dissipation. The design is further optimized using the SOI technique

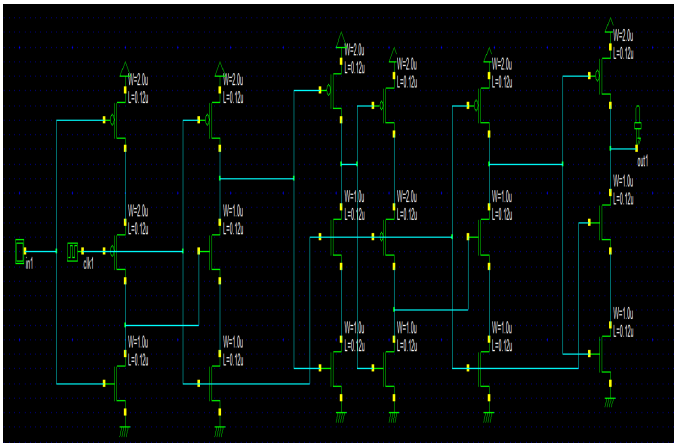

Fig 1 TSPC Synchronizer

3. LAYOUT OF THE DESIGN

Figure 2 shows the layout of the design designed in the MICROWIND software. The layout has been designed in the 120nm library. The layout has an area of 372.3 um2 and it requires 10 NMOS and 8 PMOS to design the synchronizer.

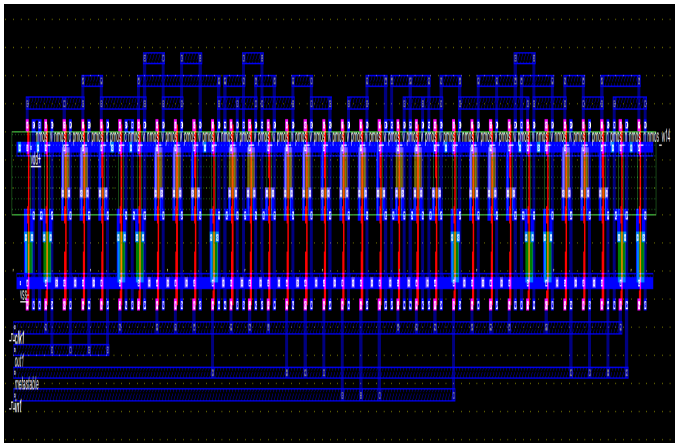

Fig 2 Layout of TSPC synchronizer

4. RESULTS

All the circuits are simulated in the 120nm CMOS and 120nm SOI library. The voltages used are vdd = 0.9 hvdd = 2.5 and temperature = 27 c. The MOSFET LEVEL 3 MODELS are used for the simulations to take into account the short channel effects. Input clock having period 32s is used with the input having the period of 40s.

Figure 3 depicts the simulation of the TSPC Synchronizer done in the MICROWIND. The rise time and fall time are 14ps and 05ps respectively. The total power dissipation is 5.173 uw.

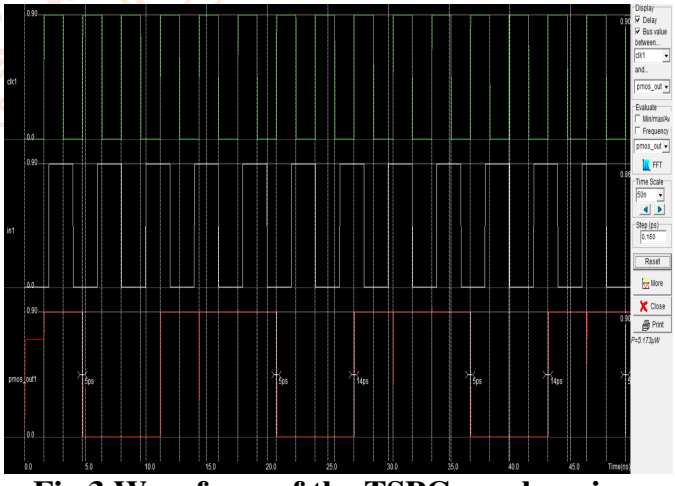

Fig 3 Waveform of the TSPC synchronizer

The performance analysis of the designed SOI based TSPC synchronizer is also presented in this section. The results that we got after the simulation have been summarized in table 1.

Table1: Summarization of the results

Digital Circuit Designing Technique	No. of Trans-Istors	Area in Um^2	Delay (Rise Time)	Delay (Fall Time)	Power Dissip-Ation in Uw	Power Delay Product
1. TSPC	18	372.3	14	5	5.173	72.422
2. C2MOS	18	444.5	18	6	7.304	131.472
3. TGMS	38	1224.7	21	35	13.356	467.46
4. GDI	38	850.5	49	40	24.68	1209.32
5. PASS TRANSISTORS	24	409.5	23	34	32.185	1094.29

Figure 4 shows the reduction in the dissipation of the power when TSPC is used in place of the existing circuit designing technique.

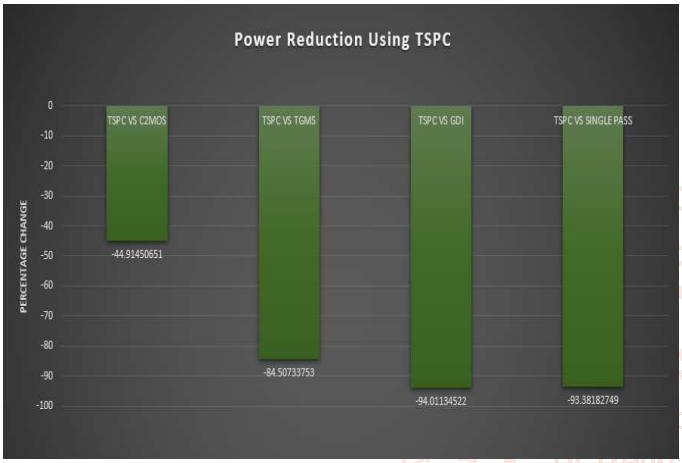

Fig 4 Power reduction using TSPC

Figure 5 depicts the reduction in the power delay product when the circuits are implemented in the SOI technique.

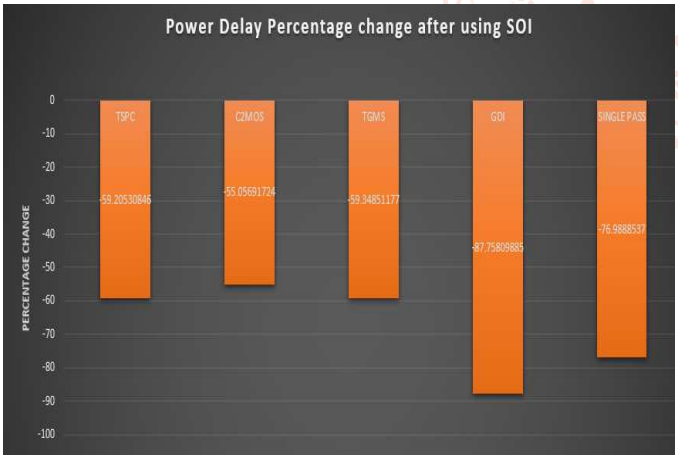

Fig 5 Power delay percentage change after using SOI

5. CONCLUSION

The complexity of designs has expanded dramatically in recent years, and as a result, we now have many components on a single chip that use independent clocks, implying that these clocks are not synchronized. As a result, Clock Domain Crossing difficulties will arise, which, if not addressed, will multiply and destroy the entire chip. Data crossing clock domains can result in a range of issues, including metastability and data loss, which can lead to the chip's full failure. As a result, we require a synchronizer that solves the CDC problem while also leveraging some unique techniques other than BULK CMOS and thereby outperforms its competitors. The synchronizer designed using TSPC proved to be the best amongst all the compared techniques. TSPC synchronizer when implemented in SOI technology gave outstanding results. It improves the rise time by 46.15 %, the fall time by 28.57 %, dissipates 24.23% less power, POWER DELAY PRODUCT by a huge margin of 59.20 % when compared to its bulk CMOS counterpart.

Hence TSPC with SOI is the best synchronizer in every aspect and therefore can be used where we require low power, delay and area on the chip. It can also be used in the High RF areas because of the usage of SOI.

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