International Journal of Trend in Scientific Research and Development (IJTSRD)
Volume 6 Issue 2, January-February 2022 Available Online: www.ijtsrd.com e-ISSN: 2456 – 6470

Review on 75-305 Ghz Power Amplifier MMIC with 10-14.9 dBm P_{out} in a 35-nm InGaAs mHEMT Technology

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ABSTRACT

The broadband power amplifier monolithic microwave ICs with an operating frequency of more than 200 GHz is demonstrated. It is fabricated in a 35-nm gate-length metamorphic high-electron-mobility transistor. The power amplifier produces a minimum output power of 10 dBm with an average value of 12.8 dBm at 75 to 305 GHz. A peak output power of 14.9 dBm and power added efficiency of 6.6% is obtained at 200 GHz.

KEYWORDS: *Metamorphic HEMT (mHEMs), Monolithic microwave integrated circuit (MMIC), power amplifier (PA,) thin-film microstrip transmission line (TFMSL), unit amplifier*

How to cite this paper: Padmam Kaimal "Review on 75-305 Ghz Power Amplifier MMIC with 10-14.9 dBm Pout in a 35-nm InGaAs mHEMT Technology" Published in International Journal of Trend in Scientific Research and Development (ijtsrd), ISSN: 2456-6470, Volume-6 | Issue-2, February 2022, pp.919-922, URL: www.ijtsrd.com/papers/ijtsrd49251.pdf

IJTSRD49251

INTRODUCTION

The research in the sub millimeter-wave frequency regime around 300 GHz for communication, radar, and imaging applications has been trending recently. The MMIC market has grown significantly over the past thirty years across various sectors. More technological advancements and requirements in the consumer electronics, such as the need for high data rates in mobile communication and to wireless infrastructure, are expected in the market growth. Metamorphic HEMT were demonstrated as Low-noise amplifiers [2] for the detection of weak signals in radio astronomy, wireless communication, radar or radiometer systems.

The presented power amplifier (PA) monolithic microwave integrated circuits (MMICs) that operate frequencies around 200 GHz and above are based on InGaAs HEMT technologies. For frequencies of about 250 GHz, the highest P_{out} was found to be 17.2–23.5 dBm for a frequency range from 182 to 265 GHz [3]. At a frequency of about 300 GHz, the maximum value of P_{out} is 10.3 to 13.8 dBm [4] In the following sections the design of the PA MMIC is discussed and the performance is measured.

A. Design of PA MMIC

The PA MMIC shown in Fig 1 is fabricated with a size of 2.25 × 0.75 mm2 without dc and RF pads. The occupied chip area is 1.5 × 0.5 mm2 without dc and RF pads [1]. The reference plane of the S-parameter measurements are indicated by the white solid lines. The unit amplifiers are highlighted by the white dashed lines.

The HEMT layers are grown by molecular beam epitaxy on 100-mm GaAs wafers. The back-end-of-line process features three interconnect gold layers each separated by a benzocyclobutene (BCB) layer. The backside process includes wafer thinning to a thickness of 50 µm and through-substrate vias[1].

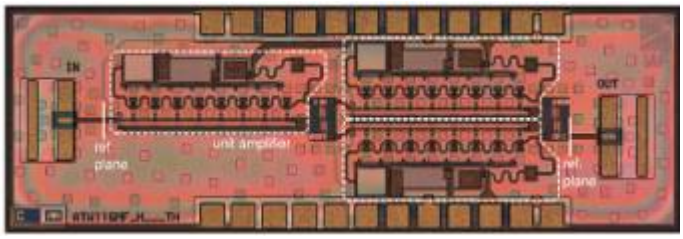

Fig 1 Photograph of the fabricated PA MMIC chip [1].

A major part of the circuit is designed with thin-film microstrip transmission lines (TFMSLs) using the first metal (MET1) interconnect layer as a ground plane. The core of the MMIC is a UA, which is based on an eight-cell distributed amplifier (DA) [7]. Each cell utilizes an RF cascode with two 2 × 10 µm HEMTs. The device size is chosen to allow the design of a DA up to an operating frequency of at least 300 GHz without capacitive division at the unit-cell input and to provide a maximum gate width for high output power. The schematic of a unit cell is illustrated in Fig. 2(a). The TFMSL between the two transistors and the capacitance at the second gate are chosen to ensure a stable operation and maximum gain. The gate bias of the second HEMT (V g2) is supplied via a 1-k resistor. The first gate is biased via the gate line of the DA. In order to avoid an asymmetric operation of the cascode, the values of the series resistors in the gate-bias paths are equal[1].

The diagram of the UA is shown in Fig. 2. The amplifier topology is based on a uniform Distributed amplifier so that there are identical unit cells. The input and output lines fhas a characteristic impedance of 62 Ω and a length of 71 and 111 µm, respectively. Finally, the input lines is terminated with a 25-Ω and output line is terminated with 60Ω resistors. The resistors are grounded through large capacitors. Through the gate-line termination resistor, the first transistor's gate bias of the unit cells are given[1].

The drain bias is supplied through an integrated bias tee at the unit amplifier's output. It comprises of two RF-shorted quarter-wave stubs that are optimized for the upper band. To decrease RF losses, the input and output lines and the bias tee use the third interconnect metal layer.

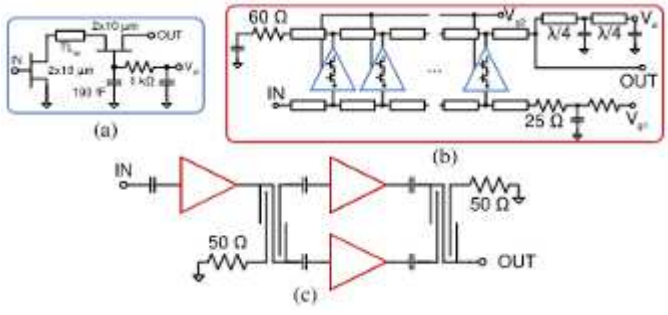

Fig 2 Block diagram of demonstrated PA MMIC of (a) unit cell of distributed amplifier(b) unit amplifier(c) whole PA

A schematic of the whole PA MMIC is shown in Fig. 2(c). Two unit amplifiers are combined at output stage in a balanced configuration. At the input of the PA, third unit amplifier is used as the driver. The four port interdigitated structure lange couplers are optimized at output stage for the upper part of the band. In the area of the Lange coupler ,the MET1 ground plane is opened. In MET1, the coupler strips are designed. The dc blocking capacitors of the input and output lines of the unit amplifier in the output stage are integrated into the space where the MET1 ground plane is opened to the lange coupler. Three advantages are offered in such aspect[1]. Firstly, the transmission lines connecting the inner part of the Lange coupler are anyway needed and, thus, offer the possibility to integrate the series capacitors with less additional losses. Secondly, RF losses can be reduced. Reducing the occupied chip area and making the PA more compact will be third advantage. The lange couplers comprises of two series blocking capacitors. So, there is no need of dc block at the output of the driver unit amplifier. A capacitor in an elevated coplanar waveguide is utilized at input of MMIC. When the integrated capacitors with the Lange coupler is used, a wider lower electrode of the capacitor is only required and that enables a larger capacitance for the equivalent length[1].

B. RESULTS

With different setups the MMIC was measured on wafer. For better comparison with the simulated results, the S-parameters are determined with respect to reference plane on-wafer that are shown by white lines in Fig. 1. For the large-signal measurements, the setups are determined with respect to the probe tips. The gate voltage of the first UA applies to all measurements It is controlled to achieve a specific drain current. The outputs of two unit amplifiers share similar gate voltages as the first unit amplifier. The gate of the upper transistors of the RF cascodes are biased for achieving symmetric drain–source voltages of both transistors. Table I shows the small- and large-signal performance measured of the demonstrated PA MMIC [1].

TABLE I. SUMMARY OF MMIC MEASUREMENTS

BW (GHz)	S_{21} (dB)	$P_{dc,PA}$ (mW)	Gt (dB)	PAE (%)	P_{out} (dBm)
75-305	>17.5*	500	>19	2-6.6	10-14.9

*For a supply voltage of 1.8 V

Using Anritsu VectorStar vector network analyzer up to 220 GHz and a Keysight PNA-X uses VDI WR3.4 waveguide extenders from 220 to 335 GHz the S-parameters are measured. Calibration is performed using multi-line thru-reflect-lines (MTRL), an

algorithm that uses a dedicated on-wafer standard. The measured and simulated S-parameters are shown in Fig. 3 with 1.8 V supply voltage and a 500 mA/mm drain current[1].

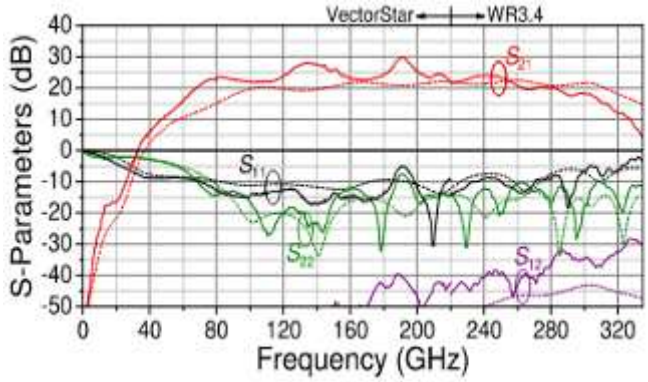

Fig 3 Measured and simulated S parameters of state-of-art PA MMIC

For the measurement of the large-signal performance of the PA the frequency ranges were of 75 to 110, 110 to 140, 140 to 215 and 225 to 325 GHz. The first setup use a Key sight signal generator and frequency multipliers as a signal source. The second setup utilizes a Keysight WR10 and an ELVA-1 WR6.5 power sensor. With a motorized waveguide attenuator the input power is controlled. The latter setups utilize Keysight PNA-X with VDI WR5.1 and WR3.4 waveguide extenders. The waveguide extenders were modified to ensure linearity at the specified power levels[1].

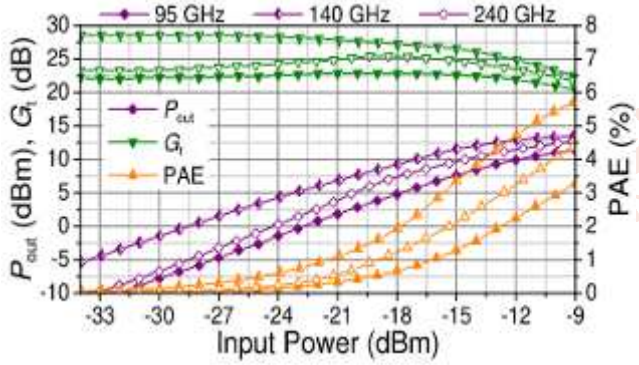

Fig.4. Pout, Gt, and PAE for an input power sweep from –34 to –9 dBm with 1.8 V supply voltage at different operating frequencies

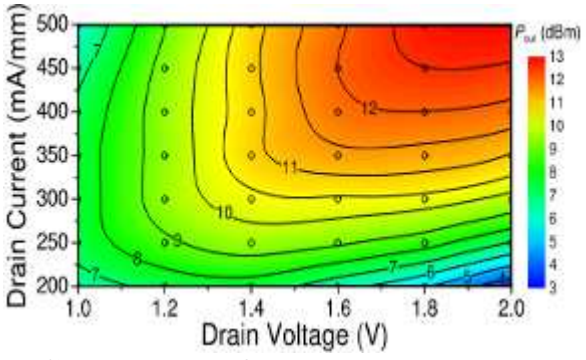

Fig 5 Contour plot of measured saturated output power at 240 GHz as a function of bias the actual measured bias is shown by black lines.

In Fig4, good performance is obtained for an input power of nearly –9 dBm with output power between 11.4 and 13.5 dBm[1].The bias dependence of the saturated output power at 240 GHz is illustrated in Fig. 5. A maximum output power is attained for a quiescent current of 500 mA/mm and a supply voltage between 1.8 and 2V [1].

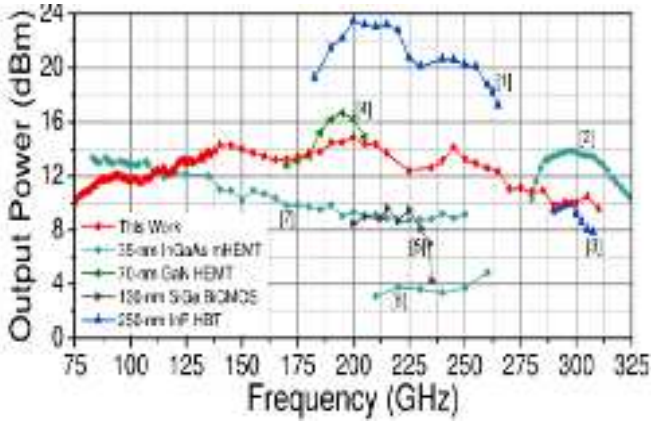

Fig 6 Comparison of different semiconductor technologies of broadband PA MMIC operating at frequency of 200GHz and above

The comparison in Fig 6 shows significant improvement in this work over wideband PA MMICs with a band-width of 75–305 GHz and an output power greater than 10 dBm. 14.9 dBm peak output power is achieved at 200 GHz. This proves the first octave-bandwidth PA MMIC having output power of 10 dBm at an operating frequency of 300 GHz[1].

Conclusion

The presented PA MMIC was designed in 35-nm gate-length InGaAs mHEMT technology.. The power amplifier produces a minimum output power of 10 dBm with an average value of 12.8 dBm at 75 to 305 GHz. A peak output power of 14.9 dBm and power added efficiency of 6.6% is obtained at 200 GHz. So, the presented work is an amazing alternative to reactively matched PAs for wideband systems at frequencies of up to 300 GHz and reveal the advantages of distributed amplifier for banded applications.

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