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THD Minimization and Fault Analysis of Modular Multilevel Converters

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ABSTRACT

Modular Multilevel Converters (M2Cs) have become an interesting topology for dc/ac conversions and vice versa showing advantages of high modularity, extensible, fault tolerant ability, high quality output and decreased harmonics. Number of converter submodules (SMs) operates in a sequence, generating multilevel output voltages and currents. This manuscript focuses on the comparative analysis of M2Cs based upon the total harmonic distortion (THD) under the application of LCL filter. The objective of filter application is to ensure that voltage harmonic distortion at the point of common coupling is less than 5%. Also, a fault monitoring scheme to detect and localize M2C SM switch failures is discussed. The presented scheme detects and localizes the fault in relatively lesser time. Simulation results are presented in order to verify results based upon the prototypes with 5, 7 and 9-level M2C.

KEYWORDS: *Modular Multilevel Converters (M2Cs), Submodules (SMs), Total Harmonic Distortion (THD)*

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I. INTRODUCTION

Starting from mid- 1970s, the idea of multilevel inverters was initiated for achieving multilevel output voltages from direct current [1]. At the first phase, dc/ac convert was main principle through CSCs usages for high power however, deficiency of power reversible ability, lesser value of efficiency, more harmonic value [2]. This culminated in the development of VSCs. A. Lesnicar and R. Marquardt introduced a converter topology acceptable for high voltage operations named Modular Multilevel Converters (M2C) in 2003[3].

In the power system these power converters behave as non-linear loads and draws harmonics and reactive power component from the AC supply. These harmonics causes distortions in load side voltages, currents, protection system and interference in nearby running communication lines [4]. For the output voltages carried out into the load, an inductor is interconnected in series between the converter output port and the load. Although, a single inductor is simple in use but offers low attenuation and makes a poor system dynamic causing a long-time response. However, for high power applications, a bulky inductive passive filter may be required which would increase the cost, losses and also reduces the effectiveness of the converter [5]. It is more advantageous to use LCL filter on comparison with the conventional L and LC filters since LCL filters show many advantages such as:1) operation at low switching frequencies, 2) lesser voltage drop, 3) better damping [6]. For determining the level of filtering required, relevant standards associated with it are IEEE 519-1992 and IEC 61000-3-12 [5].

VSIs with higher order LCL filters were considered as the appropriate solution for harmonics and ripple minimization and LCL filters being third order system are mostly preferred for high power applications [5], [7]- [8]. An experimental design method has been explored with regard to passively damping LCL filters [5]. IEEE Std. 1547-2005 and 2015 is to ensure that the voltage harmonic distortion at the PCC, is less than 5% and individual frequency voltage harmonics should not exceed 3% [9]- [10].

Generally, hundreds of switching SMs are inter-connected, so fault occurrence possibility is higher [11]. Different types of SM faults involve the following: short-circuit faults and open-circuit faults [12]. M2C operating under such failure conditions causes the capacitor of faulty SM to reach a voltage higher than that of the other healthy SM capacitors resulting in distorted output reducing the efficiency and reliability [12]. Modern IGBTs can handle a fault current which is 2-10 times the nominal value. Safety schemes related to short circuit failures are usually embedded within the gate drivers of power switching device [13]. Therefore, further analysis in this paper is only carried out on open circuit faults. In [13], localization of SM faults for M2C based upon SRM is presented. This method monitors both single or multiple switch open-circuit failures in same or different arms. A strategy based on sliding mode observer (SMO) is represented in [14], which is capable of locating a fault within a very short duration of time. This method compares actual simulated state with the observed state of M2C and differences between the two are used to detect the fault. It is robust against measurement inaccuracy, parameter uncertainty and imbalanced capacitor voltage. In [15], a Kalman filter-based fault diagnosis system is proposed where fault detection is carried out based upon inner difference current value and capacitor voltage difference between healthy and faulty SM is noticed for fault localization. However, it does not take long to complete the fault diagnosis procedure, taking an average time of 100ms**.** The method in [16] emphasizes that open-circuit as well as short-circuit failures in M2C are founded and localized. The limitation of whole M2C is more important as compared to SM fault which can occur because of mal-operation of failure system [17]. A system of optimized hand may handle the current is given to create maximum application of successful SM's and the power ability to larger extent as possible [18], which reduces the failed SM's and controls the non-failure SMs. Several fault diagnoses schemes have been implemented locating the fault position within a short time of 50 ms to 150ms [19]. With low computation burden, extended state observers (ESO) strategy for fault monitoring featuring faster fault detection and localization without assumption check process is discussed in [19]. The above-mentioned fault diagnosis schemes engage in complex designs and calculations to first detect the M2C fault, further identifying the faulty SM by going through the internal dynamics of M2C, thus taking longer time to locate the fault.

This paper follows as: Structure of M2C is discussed in section 2. The basic principle is explained in section 3. Section 4 discusses about the M2C with LCL filter. Fault analysis and monitoring is explained in section 5 and 6. In section 7, the simulation outcomes are presented. In section 8, a conclusion based on THD minimization and fault analysis of M2C has been drawn.

II. Methodology

Modular Multilevel Converters (M2Cs) methodology is used. Based upon the operating principle, large number of converter modules operate in a sequence, generating multilevel output voltages and currents. Modular multilevel converters differ from conventional multilevel converters because of its modular structure having series connected half-bridge SMs and having the capability of controlled power exchange, lesser radio interference, lower corona losses in High Voltage Direct Current (HVDC) systems which makes it more advantageous.

III. Structure of M2C

Figure 1 shows a 3-phase M2C with different SMs connected. Each SM comprises of two controlled power switching devices and a capacitor.

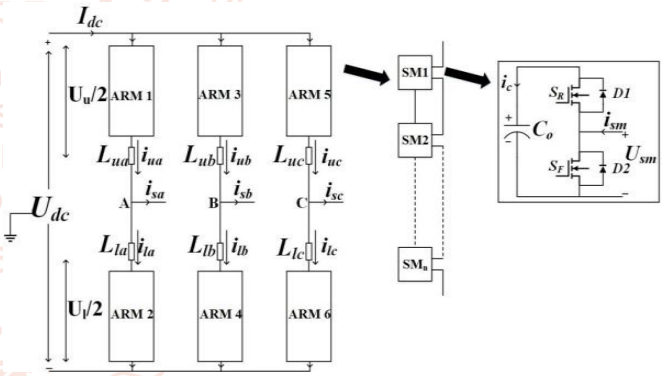

Figure 1: Schematic diagram of a three-phase M2C with SM unit.

U_{dc} and I_{dc} represent the DC input voltage and current for M2C; upper as well as lower arm currents are showed through the symbol of i_{ua} and i_{la} for phase A; L_{ua} and L_{la} represents the limiting current reactance for upper as well as lower hand of stage A for reducing the current changes respectively; U_u and U_l represents the upper as well as lower hand of voltages;i_{sa} , i_{sb} , i_{sc} shows the AC output currents; the M2CSM structure represents two controlled switches and a capacitance; i_{sm} and U_{sm} represents the terminal current and voltage; U_c, i_c represents the capacitor voltage and current respectively.

IV. Operating principle of M2C

When the current i_{sm} enters the SM, it is denoted by $i_{sm} > 0$; when the current ism leaves the SM, it is denoted by $i_{sm} < 0$. The control states of a SM

based upon current (i_{sm}) direction are explained in table 1.

Table 1: Control states of a SUBMODULE.

SM current direction(i_{sm})	S_R	S_F	SM capacitor C_0	Terminal voltage (U_{sm})
(I) >0	ON	OFF	charging	U_C
(II) >0	OFF	ON	bypass	0
(III) <0	ON	OFF	discharging	U_C
(IV) <0	OFF	ON	bypass	0

V. M2C with LCL filter

Figure 2 shows the M2C connected to a 3-phase load through a LCL filter. *L1* is connected to the inverter side, *L2* connected to the load side and capacitor C connected to the ground as shown.

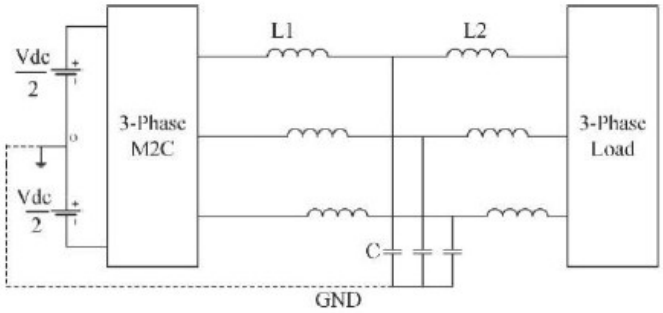

Figure 2:M2C-Load connection through LCL filter.

VI. Behaviour of M2C under IGBT failures

Two kinds of open-circuit defaults include: (a) S_F failure, (b) S_R failure. These defaults can or cannot influence the parameters of output of M2C which depends on the direction of current.

(a)Characteristics of S_R open-circuit failure

The features of S_R failure are explained in table 2.

Table 2: S_R open circuit failure characteristics.

SM current direction (i_{sm})	Command	Healthy conditions	S_R open circuit failure
(I) >0	inserted	C_0charging	C_0 charging
(II) >0	bypassed	unchanged	unchanged
(III) <0	**inserted**	**C_0 discharging**	**unchanged**
(IV) <0	bypassed	unchanged	unchanged

(b)Characteristics of S_F open-circuit failure

The features of S_F failure are enlisted in table 3.

Table 3: S_F open circuit failure characteristics.

SM current direction (i_{sm})	Command	Healthy conditions	S_F open circuit failure
(I) >0	inserted	C_0charging	C_0 charging
(II) >0	**bypassed**	**unchanged**	**C_0 charging**
(III) <0	inserted	C_0 discharging	C_0 discharging
(IV) <0	bypassed	unchanged	unchanged

VII. Fault monitoring technique of M2C

The principle of proposed fault monitoring technique for $_{iarm}$>0 is illustrated in figure 3.

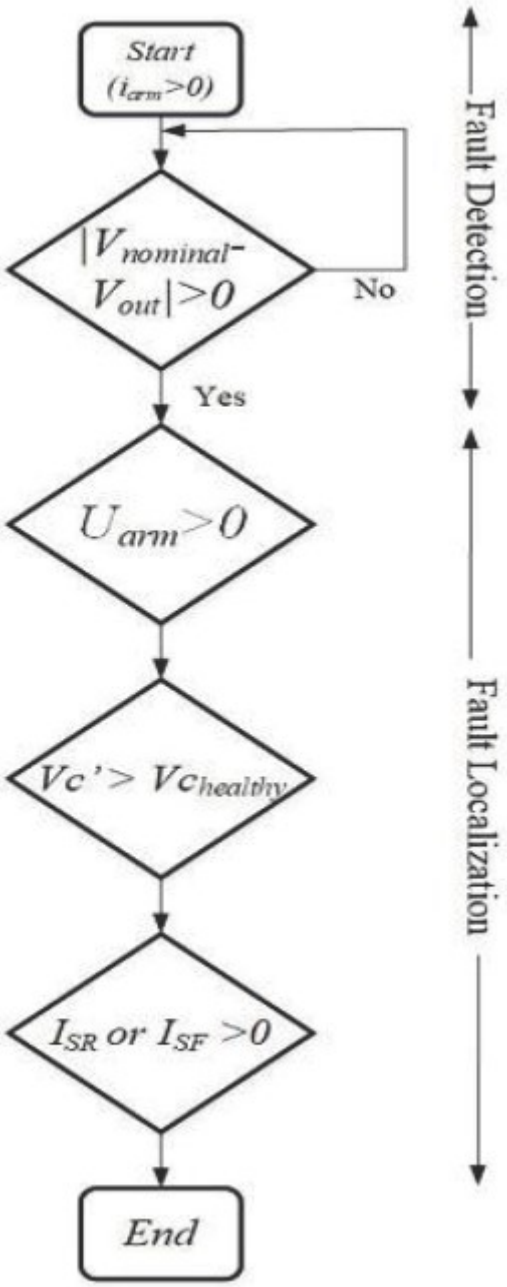

Figure 3: Flow chart of proposed fault detection and localization method.

During failure, the actual or observed peak output voltage (V_{out}) would be different from the theoretical or nominal peak value ($V_{nominal}$), thus detecting the fault. Arm voltage (U_{arm}) is the individual sum of SM terminal voltages either of upper or lower arm.

During S_R failure and i_{sm}<0, the observed arm voltage value is lesser than the nominal value. During S_F failure and i_{sm}>0, the nominal arm voltage is lesser than the observed value and switch body diode stays in conduction for all time. The difference between nominal and actual arm voltage would be positive for SR fault and negative for S_F fault. Fault localization is carried in following steps: (i) initially the arm voltages are compared with zero reference value and arm showing voltage levels other than zero is further analyzed for faulty module localization, (ii) faulty leg capacitor voltages are compared and the faulty SM capacitor voltage (V_C') would be higher as compared with other capacitor voltages ($V_{chealthy}$) of healthy SM within the same leg, (iii)further, for faulty switch localization switch currents (I_{SR} or I_{SF}) could be analysed and compared with zero reference. Switch showing non-zero switching current is faulty. This method of fault detection and localization is applied only for single IGBT open circuit failures. However, in real application, a current sensor per switch could be used to sense the over current thus, operating SM faulty switch accordingly.

VIII. Results

In this section, a comparative analysis of 3-phase 5-level and 7-level M2C with LCL filter under different frequency levels based upon THD is illustrated. Fault analysis is carried out under 9-level M2C by monitoring the arm voltages, rate of change of SM capacitor voltages and load current. The given model structures are made in MATLAB (R2015a) with system configuration parameters as listed in table 4.

Table 4: System configuration parameters.

M2C parameters	
Supply Voltage (V_{DC})	100V
Switching Frequency *fsw1* (5-level)	83.33Hz
fsw2 (7-level)	62.5Hz
fsw3(9-level)	50Hz
Initial SM capacitor voltage ($Vc-$)	50V
LCL filter parameters	
Converter side inductor ($L1$)	0.07H
Filter capacitance (C)	200μF
Load side inductor ($L2$)	0.07H
Load parameters	
Resistive Load-RL	10000Ω
Inductive Load-LL	1H

(a) THD analysis

5-level M2C

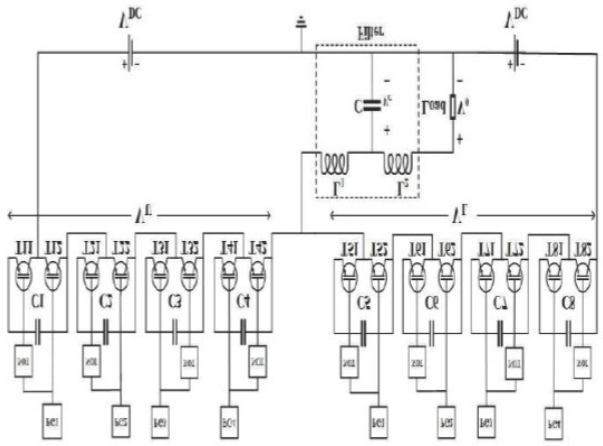

Figure 4: Proposed 5-level M2C model with LCL filter.

Figure 4 represents the simulink model of the proposed single phase 5-level M2C with 4 upper and 4 lower arm SMs. C1-C4 and C5-C8 are the upper as well as lower leg SM capacitors. V_U as well as V_L represents the upper and lower leg voltages respectively. T11-T42 and T51-T82 represents the SM IGBTs of the upper as well as lower leg. The turn ON and OFF of SM IGBTs are controlled by pulse generators PG1-PG4. The load voltage V_0 is measured in between the midpoint of the phase leg and ground as shown.

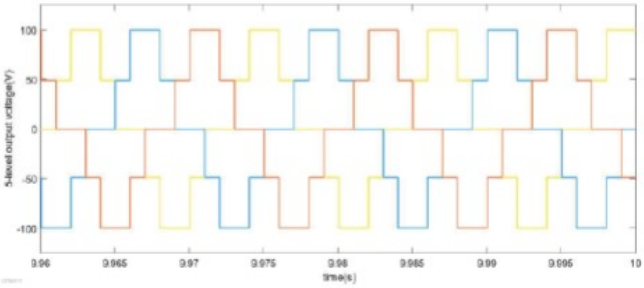

Figure 5: Three phase 5-stepped output voltage.

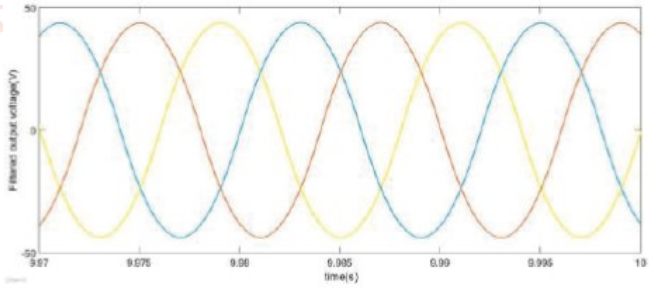

Figure 6: Sinusoidal 3-phase output voltage for 5-level M2C with LCL filter.

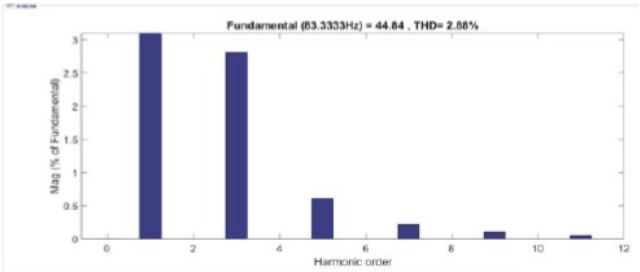

Figure 7: Harmonic spectrum for 5-level M2C with *LCL* filter.

Figure 5 represents the three-phase 5-stepped voltage at the output terminals showing voltage levels varying from -100V to 0V to 100V under steady state. Figure 6 represents the sinusoidal 3-phase output voltage measured at the output port of *LCL* filter. Peak value of output voltage is 43.7V and frequency is 83.33Hz. Figure 7 represents the harmonic spectrum analyzing the total harmonic distortion under resistive-inductive load. At the frequency of 83.33Hz the total harmonic distortion is 32.88% with respect to fundamental. Figure 8 represents the harmonic spectrum analyzing the total harmonic distortion of sinusoidal 3-phase output voltage. At the frequency of 83.33Hz the total harmonic distortion is 2.88% with respect to fundamental.

(b) Fault analysis of 9-level M2C The simulation was taken and different voltage levels -100V to +100V under safe operation are observed.

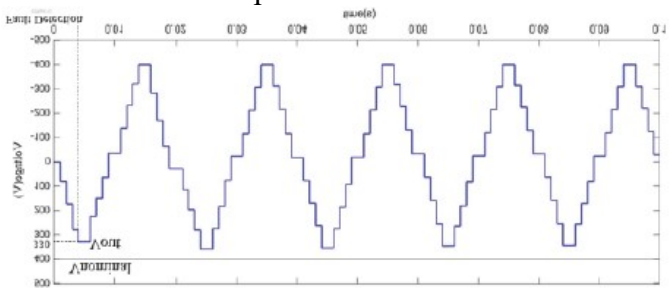

Figure 8: 9-stepped output current waveform under open-circuit failure conditions.

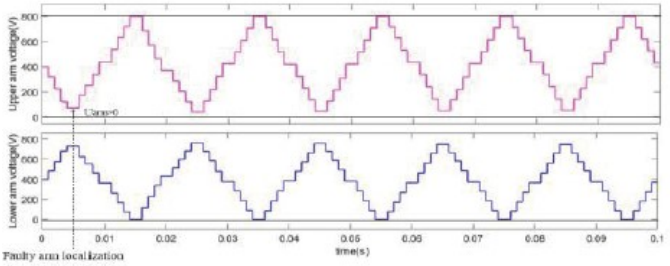

Figure 9: Upper arm and lower arm voltages under faulty conditions.

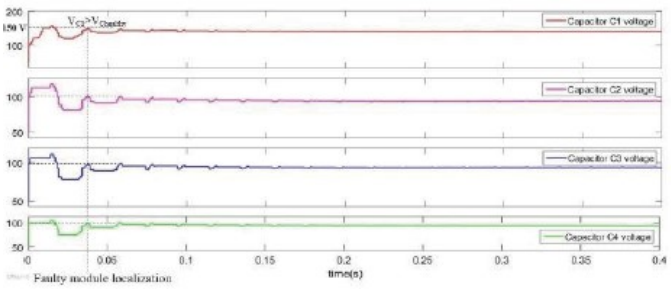

Figure 10: Capacitor voltages under faulty conditions (C1-C4).

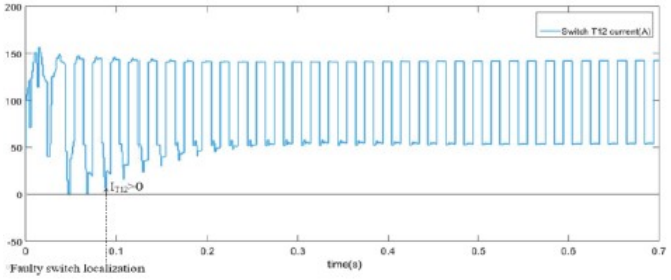

Figure 11: Faulty IGBT T12 current.

Figure 8 illustrates the output voltage waveform under open circuit fault conditions and defines that peak voltage value drops to 330V in 4.5milliseconds of operation. Figure 9 illustrates the upper and lower leg voltages under faulty conditions and it was observed that the upper leg voltage shows deviation from the nominal and waveform shifts above from the zero level, thereby localizing the faulty arm. So, the further analysis was carried out on upper arm of M2C. Further, for faulty module localization, rate of change of module capacitor voltages are observed and compared. The voltage of faulty module capacitor will be much higher as compared to the SM capacitors. From figure 10, it was cleared that the faulty SM capacitor voltage reaches to a voltage level of 150Vin 0.04 seconds while the healthy SM capacitors maintain the voltage level of 100V before fault, during fault and after clearing fault. For localizing the faulty switch, the faulty module IGBT currents are observed. From figure 11, it was presented that switch T12 body diode remains in conduction for time above 0.09 second and allows current level of 140A under steady state which was higher than the nominal value, thereby localizing the faulty IGBT.

IX. Conclusion

Table 5: Comparison of THD for different M2Cs with LCL filter.

Level	THD
5-level	2.88%
7-level	1.13%
9-level	0.45%

In this paper, comparative analysis of 3-phase 5-level,7-level and 9-level M2Cs with LCL filtering based upon THD is illustrated. Table 5 shows the comparison results for the proposed M2Cs at different frequency levels. Proposed THD results are in accordance with the IEEE Std. 1547-2005 and 2015 with less than 5% voltage harmonic distortion. Also, a general and straight forward method for fault detection and localizations is proposed in detail. The presented scheme detects and localizes the fault in 85 to 90 milliseconds which is relatively faster.

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