Design of Low Power Dynamic Comparator using Reversible Logic

Mounica. E[1], Saranya. B[1], Shanmika. K[1], Balakumaran. D[2]

[2]Assistant Professor,

[1,2]Department of Electronics and Communication Engineering,

[1,2]S.A. Engineering College, Thiruverkadu, Tamil Nadu, India

ABSTRACT

The Performance of circuits based in CMOS transistor logic is close to reaching its limit. A new efficient system or technology is needed to provide solutions to computing and integration issue. The proposed work addresses the above circumstance by implementing the reversible logic in dynamic comparator so that the number of transistors can be reduced. This logic can also be implemented in order to lower the power consumption and improve performance of circuit. The inputs and outputs of reversible logic gates can be uniquely retrievable from each other. The proposed reversible ripple carry adder is designed using L and M gates which requires only 18 transistors while the number of transistor implemented in CMOS implementation is 20. The critical path is made minimal so that the routing is reduced which makes the delays negligible. Reversible computing has its applications in computer security and transaction processing and also in those areas which require high energy efficiency, speed and performance.

KEYWORDS: Comparator, Delay effects, Reversible Logic gates, High performance computing, Logic circuits, Power dissipation

1. INTRODUCTION

The Reversible logic has become one of the most optimistic research areas in the past few decades and has its applications in several technologies. In recent years, Reversible logic has gained great attention in recent years due to their ability to reduce the power dissipation which is the essential requirement in low power VLSI design. It is applied in areas such as low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. Information loss leads to energy dissipation in Irreversible hardware computation. For every irreversible bit operation The amount of energy dissipated is at least KTln2 joules, where K=1.3806505* 10-23 m2 kg-2K-1(joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1].

Due to the loss of one bit of information the heat generated is very small at room temperature but when the number of bits is high as in the case of high speed computation works the heat dissipated by them will be so large that it affects the performance and reduces the lifetime of the components. Bennett showed that energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs. The process of running the system both forward and backward is supported by reversible logic. Which means that inputs can be generated from out- puts reversible computations and also can stop and go back to any point in the computation history. If the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments then a circuit is said to be reversible, (i.e.) not only the inputs can be recovered from the outputs, but also the outputs can be uniquely determined from the inputs. If computation becomes Information-lossless energy dissipation can be reduced or even eliminated [2].

2. Reversible Computing

In current scenario, the reversible logic design attracts more interest due to its reduced power consumption. Reversible logic is very essential in low- . Reversibility information about the computational states can ever be lost, so we can recover any initial stage by computing backwards or un-computing the results. This is termed as logical reversibility. Only after employing physical reversibility, the benefits of logical reversibility can be gained. Physical reversibility is a process in which no energy is dissipated to heat. Absolutely perfect physical reversibility is practically unachievable. Heat is given off the computing systems when voltage levels change from positive to negative bits from zero to one. The energy ne eded to make that change is mostly given off in the form of heat. Instead of changing voltages to new levels,

reversible circuit elements will gradually move charge from one node to the next. By implementing the above method, one can only expect to lose a minute amount of energy on each transition. Digital logic designs are strongly affected by reversible computing. In order to recover the state of inputs from the outputs, reversible logic elements are needed. It will impact high-level programming languages and instruction sets as well. Gradually, these will also have to be reversible to provide optimal efficiency [3].

2.1. Motivation behind Reversible Logic

High-performance chips releasing large amounts of heat impose a practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by un-computing bits instead of throwing them away will soon offer the only physically possible way to keep Reversible computing will also lead to an improvement in energy efficiency. Energy efficiency will potentially affect the speed of circuits such as Nano-circuits and also affect the speed of most computing applications. In order to increase the portability of devices again, reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become portable. In spite of the high hardware design costs which may incur in near future, the power cost and the need of reversible computing cannot be ignored since the logic hardware cost in today's computing era lags behind the current performance [4] The digital computer program frequently performs operations that seem to throw away details about the computer's history, leaving the machine in a state whose immediate predecessor is equivocal. Such operations include entry into a portion of the program addressed by several different transfer instructions and erasure or overwriting of data. In other words, the model computer is logically irreversible when its transition function (if the state has a successor the partial function that maps each whole-machine state onto its successor) lacks a single-value-used inverse. Always an irreversible computer can be made reversible by having it save all the information otherwise it would throw away [4].

3. Comparator Design

A **digital or magnitude comparator** is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. **Comparators** are used in central processing unit and microcontrollers.

Fig 3.1 One bit comparator

A_0	B_0	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Table 3.1.1 The truth table for a 1-bit comparator

Dynamic Comparator

Due to its low power consumption and fast speed dynamic comparators are widely used in high-speed ADCs. Generally they use positive feedback mechanism with two pair of back-to-back cross coupled inverter to convert a small input-voltage difference to a full- scale **digital** level in a very short time low leakage current.
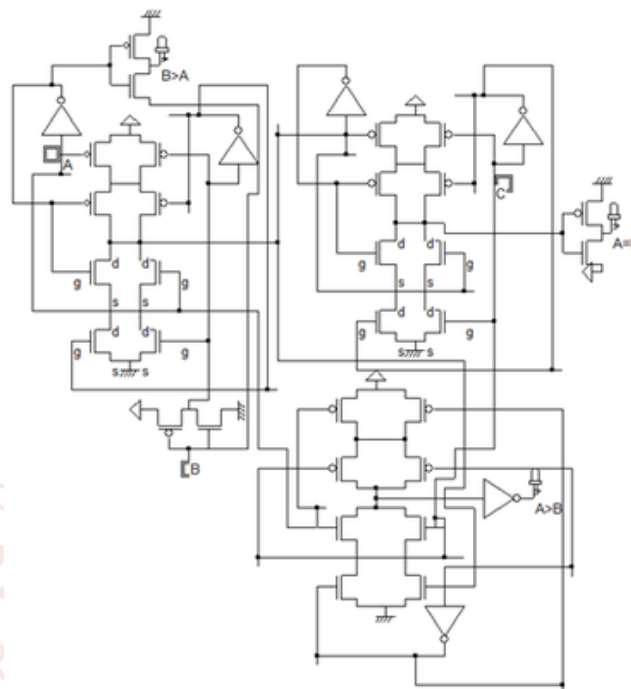

Fig.3 2 Conventional CMOS dynamic comparator Circuit

$$A0 < B0: L = \overline{A0}\ B0$$

$$A0 = B0: E = \overline{A0}\ \overline{B0} + A0\ B0$$

$$A0 > B0: G = A0\ \overline{B0}$$

It is to be noted that E can be realized as $\overline{(L + G)}$.

By using these Boolean expressions, we can implement a logic circuit for this comparator using two AND gates, one NOT gate and one Ex-NOR gate as shown in below figure. AND gates are used to find whether a binary digit is less than greater than another bit whereas Ex-NOR gate is used to find whether two binary numbers are equal or not.

In the figure, one AND gate has inputs of A0 (B0)¯and another has inputs (A0)¯B0. Therefore, one AND gate output is 1 if A0 > B0 (i.e., A0 =1 and B0 =0) and is zero if A0 < B0 (i.e., A0 =0 and B0 =1). Similarly, other AND gate output is one if A0 < B0 (i.e., A0 =0 and B0 =1) and is zero if A0 > B0 (i.e., A0 =1and B0 =0).

4. Existing Reversible Logic Circuit

Reversible one bit comparator is implemented with Feynman gate and Fred kin gate and BJN gate is as shown in fig.15. G1 to G6 were represented as number of garbage outputs, it uses seven constant inputs, four logic '0' and three logic '1'. In the input part Two Feynman gates are used for fan-out purpose. G1 and G2 were represented as garbage output it uses three constant inputs, one logic '0' and two

login '1' it requires one Feynman gate and two Toffoli gate. Performance parameters like area, power and speed. For complex gates with large fan-ins CMOS design style is not area- efficient.
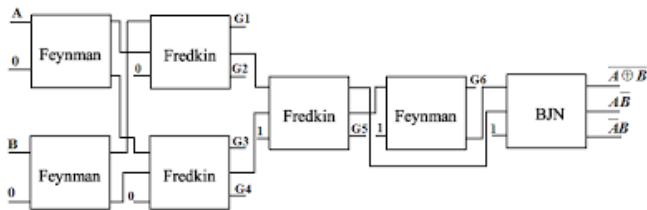

Fig 3 Reversible dynamic comparator Circuit using Fredkin Gate, BJN Gate and Feynman Gate

Drawbacks of Existing System
The circuitry is quite complex and the design is larger in size due to the transistors count. The power dissipation of the gates used are comparatively high. The power dissipation may occur mostly due to the transistor implemented and also due to information loss between the input and the output. The garbage values produced are high. The Quantum Cost of the circuit is also relatively high.

5. Proposed Comparator Design
The proposed system is designed using reversible logic by implementing reversible logic gates such as L gate and M gates. This system provides high performance and optimal power consumption than the existing systems. The proposed design is given by, constructed from it.
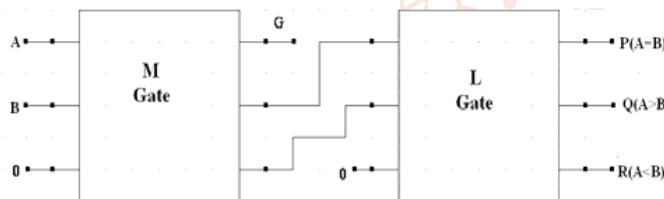
Toffoli gate is a 3x3 reversible gate having a quantum cost equivalent to five. This gate has 3-bit inputs and outputs in which if the first two bits are set, it flips the third bit [6].

5.1. M Gate
The logic diagram and truth table of the proposed Reversible M gate is as shown in the Fig 7 and Table 1. M Gate which is 3*3 gate with inputs (A, B, C) and outputs P,Q, R
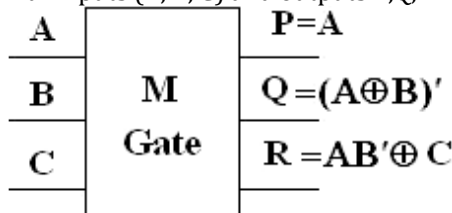
A, B, C as inputs for M gate and Produce output as P, Q, R and corresponding functionalities shown in Fig.7. Using GDI technique the transistor implementation of M gate is shown in Fig
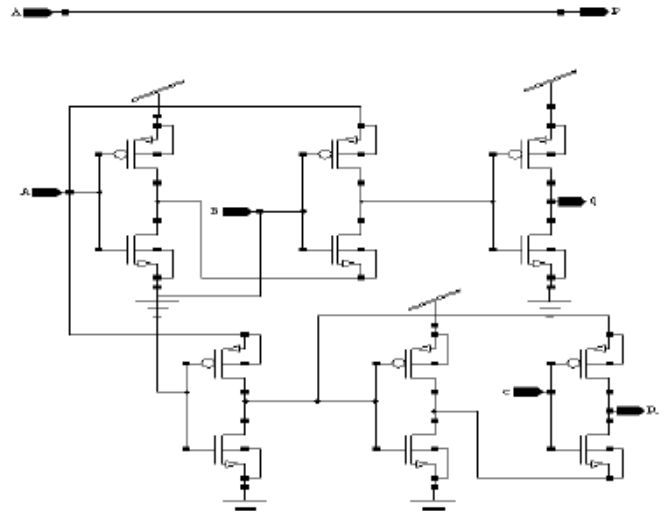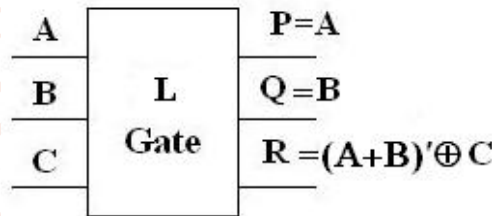

Fig 5.1 Transistor implementation of proposed M gate

5.2. L Gate
The proposed new Reversible L gates' logic diagram and truth table were shown in the Fig 8 and Table 2. L Gate which is a 3*3 gate with inputs A, B, C and outputs P, Q, R.

The L gate takes inputs as A, B, C and Produce P, Q, R as outputs and corresponding functionalities shown in Fig.8. Using GDI technique the transistor implementation of L gate is shown in Fig
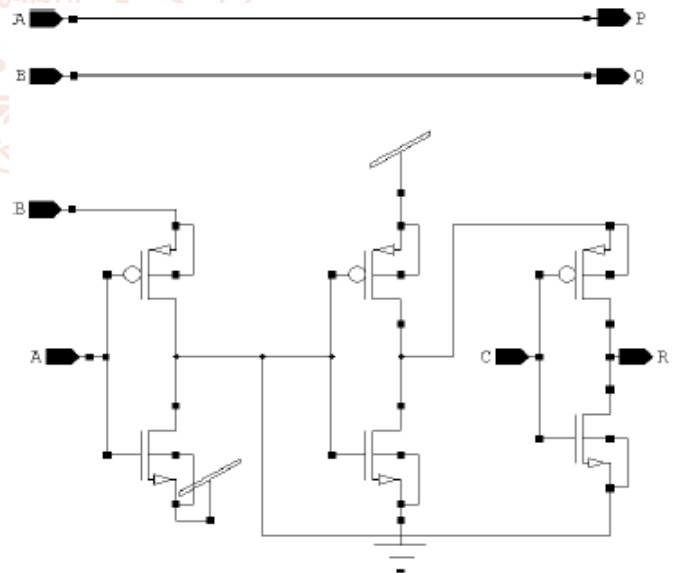

Fig 5.2 Transistor implementation of proposed L gate

6. Advantages of Proposed system
The transistor requirement in the proposed design is very minimal when compared to the other existing systems. They also consume comparatively less power due to the transistor requirement. The garbage values produced is also reduced to some extent. The power dissipation is also less since there is no information loss between the input and output sides.

They are comparatively compact and simple than the existing systems.

Table 6.1 Parametric Analysis Reversible Logic Gates

Reversible gate	No of transistors required	W/L of transistor	Voltage applied (V)	Power dissipation (watts)
M gate	12	2u/10u	5	96.764 p
			3	34.128 p
			1.5	8.1648 p
L gate	06	2u/10u	5	145.684 p
			3	51.381 p
			1.5	12.292 p

Table 6.2 Delay and Power Comparison

Parameter	Existing Dynamic Comparator	Proposed Reversible Dynamic Comparator
DELAY	51 ns	40 ns
POWER	2 µW	60 nw

The garbage values produced is also reduced to some extent. The power dissipation is also less since there is no information loss between the input and output sides. They are comparatively compact and simple than the existing systems.

Implementation of Comparator Design

The design implementation is done with the Cadence Virtuoso Schematic Editor. The steps involved in the design process are moving from the specification at the start, to a plan that contains all the information needed to be physically constructed at the end and this normally happens by passing through a number of stages, although in a very simple circuit it may be done in a single step. The process normally is initiated with the conversion of the specification into a block diagram along with the functions that the circuit must perform, at this stage the contents of each block are not necessary, only what each block must do, this is approach is referred to as a "black box" design. This approach breaks the very complicated task into smaller tasks which may either be tackled in sequence or divided amongst members of a design team.

Even though each block is considered still at an abstract stage, a lot more focus on the details of the electrical functions needs to be provided. At this or later stages it requires a large amount of mathematical model-ling into what is and is not feasible to achieve. At the earlier stages of the design process, the results of this research may be fed back to it. At this point, it is also common to start considering both how to demonstrate that the design does meet the specifications, and along with its testing process. In order to carry out each function in the overall design and the physical layout, this section the individual circuit components are chosen and electrical connections of each component are also decided, this layout commonly takes the form of artwork for the production of a printed circuit board or Integrated circuit. This stage is extremely time-consuming because of the vast array of choices. At this stage, a practical constraint on the design of standardization, while a certain value of component may be calculated for use in some location in a circuit. One essential area of rapid technology development is in the field of Nano electronic circuit design. Proper design structure and philosophy incorporates economic and technical considerations and keeps them in balance in all terms and right from the start [7].
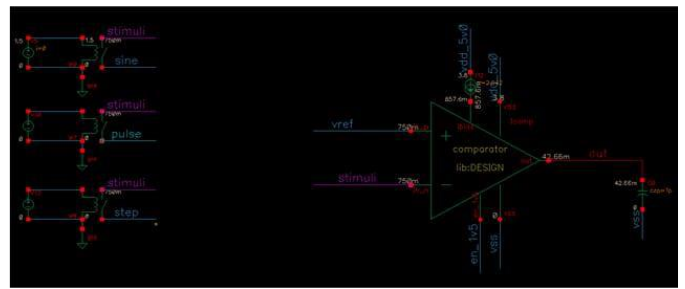

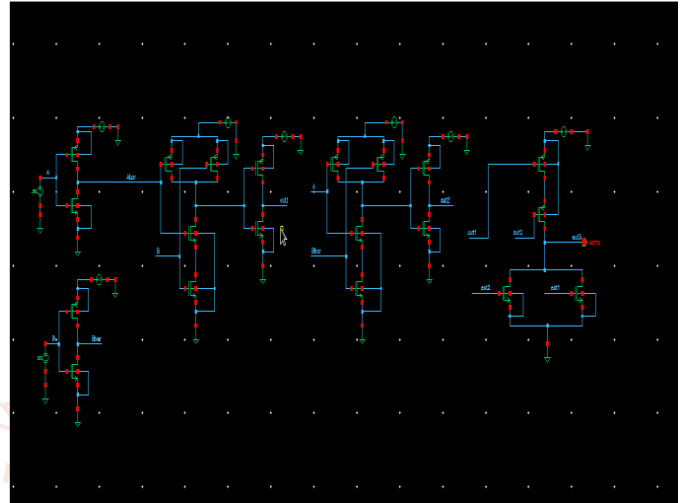**Fig 6.1 Design of dynamic comparator**

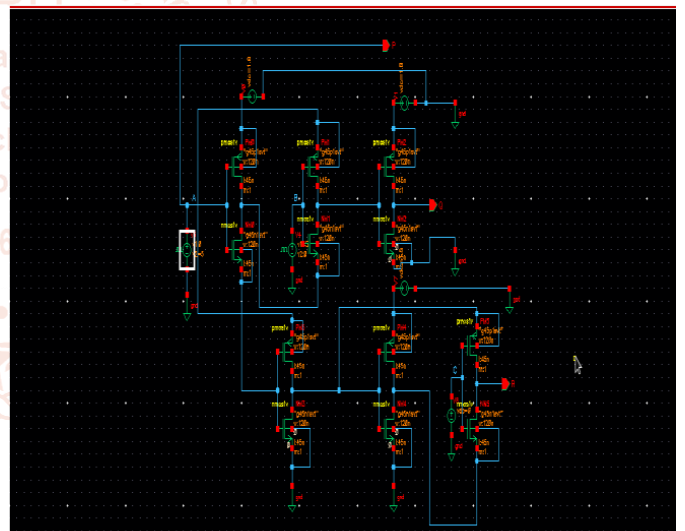**Fig 6.1.1 Transistor Implementation of Dynamic Comparator**

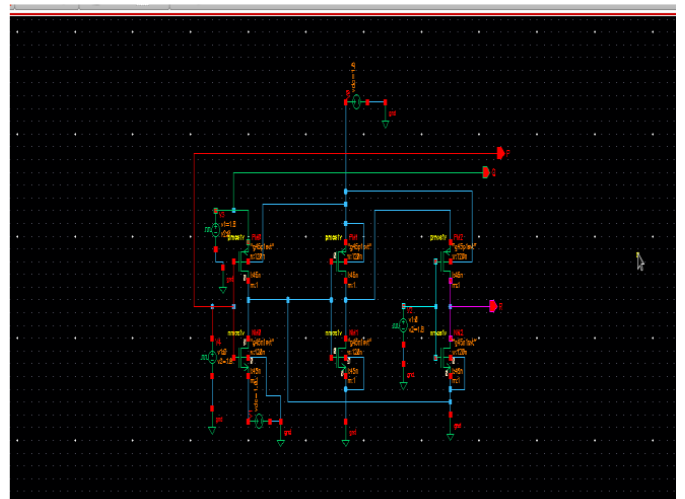**Fig 5.1.1 Transistor Implementation of M gate**

Fig 5.2.1 Transistor Implementation of L gate

Simulation Results

The proposed system is simulated by means of the Cadence Spectre Circuit Simulator. After designing a circuit, it must be both verified and tested. Verification is the process in which each stage of design is studied and ensured that it will do what the specification requires it to do. This can be a highly mathematical process and can also involve large-scale computer simulations of the design. In any complicated design, it is very common that problems will be found at this stage and may involve a large amount of the design work be rectified. Prototyping is a way of exploring ideas before an investment is made in those ideas. the project depending on the scope of the prototype and the level of detail required. Sometimes they are created during the planning and specification phase or early in the project, commonly using a process known as bread-boarding; that's when the time investment needed is most viable and when the need for exploration is greatest. Further, in the cycle packaging, mock-ups are used to explore usability and appearance.

Thus using the reversible logic the number of transistor to design a dynamic comparator is reduced to 18 transistors, which usually requires 36 transistors when design with CMOS implementation logic. Though, none of this logic can compete with CMOS style in robustness and stability, It has great improvements in terms performance and power consumption characteristics. Normally dynamic comparator designed with CMOS logic has a delay of 192 ms and power dissipation of 200 respectively.
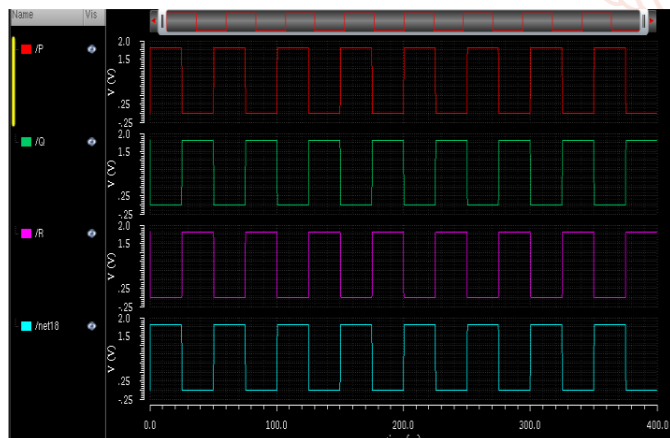

Fig 5.2.2 Stimulation of L gate

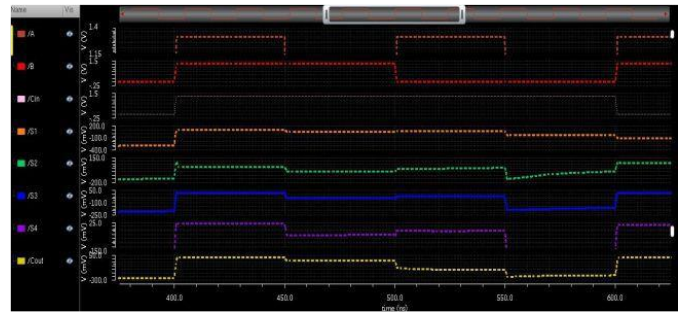**Fig 5.1.2 Stimulation of M gate**

Fig 6.1.2 Stimulation of Dynamic comparator

7. Conclusion

In applications such as VLSI, comparator circuit plays an important role. Such comparators should be designed in order to reduce the propagation delay occurring within the circuit. The main objective of this work is to reduce the transistors count in the dynamic comparator so that the performance and power consumption parameters are improved. Since the transistors requirement is less, the cost of production will be reduced and the circuit can also be made less complex and more compact.

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