High Performance Triplex Adder Using CNTFET

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ABSTRACT

Carbon Nanotubes Field Effect Transistors (CNTFETs) is used to implement a two new design of triplex half adder. Conventional binary logic has a capable alternate called triplex logic, since it is possible to accomplish uncomplicatedness and energy efficiency in modern digital design due to shortened circuit overhead such as interconnect and chip area. Triplex decoders and binary logic gates are used to present two novel half adders. To obtain power, delay and power delay product the circuits are simulated using HSPICE. Recently reported designs are compared with these circuits. These triplex adders show delay and power advantage up to 40 and 39 % with less transistor count. So, using these half adders in complex arithmetic circuits will be advantageous.

Keywords: Carbon Nano Tube, Adder, Field Effect Transistor, Logic Gates

I. INTRODUCTION

The scalability property of MOS transistors helps it to achieve its great success, which results in healthier performance. This trend still continues in harmony with Moore's law, in last few decades' silicon-based technology has gone through a impressive growth. However, MOSFET is approaching the limiting size as it is entering into the sub-nanometer regime. For this reason, the semiconductor industry is looking for different materials and devices to integrate with the current silicon-based technology and, in the long run, possibly replace it. Due to its unique structures and excellent physical properties, Carbon nanotube (CNT) has attracted significant attention in the field of electronics for the last few decades [1]–[8]. Currently, use of Carbon Nano tube has been used in the new channel of field effect transistor and obtained a new device called carbon nanotube field effect transistor (CNTFET). In 1998 [9] it was first demonstrated. Due to high electron mobility, near ballistic transport, high mechanical and thermal stability of CNT, CNTFET became one of the most promising candidates for post- silicon electronics [10]–[13].

Nowadays, many studies are going on for scheming and travelling the application of CNTFET in logic gates and analyzing its performance advantage over the existing metallic oxide semiconductor technology. Binary logic gates [6], [14]–[17], triplex logic gate [5], triplex and binary memory cells [7], [16], and multi-valued logics [8], [18] are included in the CNTFET circuit application. The application of CNTFET for multi-valued logic is of powerful interest as the threshold voltage of the CNTFET can be controlled by proper selection of the chiral vector of the CNT.

Triplex logic allows more information than binary logic to be transmitted over a given set of lines or stored for a given register length therefore it reduces the complexity of interconnects and achieving simplicity and energy effectiveness in digital design [5]. Addition of bits is done by basic digital adder circuits and the half adder adds two single binary digits A and B. adder has two outputs, sum (S) and

carry (C). The carry signal denotes an overflow into the next digit of a multi-digit addition. They disperse lots of energy, increase response time and cause coupling effects by adding more capacitance, resistance, inductance to a circuit. Multiple-valued logic (MVL) is an alternative solution to interconnect complexity and growing power dissipated by wires. Wires inside the chip are reduced. Outside a chip dramatically as more complex designs require a large number of wires for connecting circuit components [5].

In the new work two new circuits are proposed for triplex half adder circuit to have better act. The reported circuits give delay and power advantages up to 40% and 39 % with less transistor count in comparison to other work. Basic of multiple value logics and more definitely triplex logic is discussed in section II. The CNTFET's suitability for triplex logic are discussed in section III. Some basic logic gates and the previously best reported half adders are discussed in section IV. Our proposed circuits, their implementation and comparisons with other reported circuits are analyzed in section V. The final concluding remark is given in section VI.

II.   MULTIPLE VALUED LOGIC REVIEW

Multiple-valued logic (MVL) uses more than two values in contrast to the binary digital computation and it is performed using only two possible values (0 or 1, true or false). Nowadays, multiple-valued logic, such as triplex logic (or three-valued logic), has attracted considerable interests due to its budding advantages over binary logic for crafty digital systems. Requirement of less memory, less interconnections and reduction of chip area, high bandwidth parallel, serial data transfer, high potential for increasing computational   speed and reducing switching   activity   and employment of many arithmetic and logic functions in a single chip are some of the benefits of MVL.

Among many Multi valued logic systems, triplex logic (also known as three-valued logic) has been of more interest than any other due to its simplicity and efficiency. In this work we have focused on triplex logic which is Multi valued logic with three levels.

Triplex Logic (Three-valued logic): Triplex logic functions include a third value in addition to the binary logic. In this 0, 1, and 2 are used in triplex logic to symbolize the triplex values false, undefined, and true, respectively. Any n variable $\{X_1, \ldots ,X_n \}$ triplex function f(X) is called as a logic function plotting $\{0, 1, 2\}^n$ to $\{0, 1, 2\}$, where $X = \{X_1, \ldots , X_n\}$ [5]. Advantages of triplex logic are:

1.   The number of required computational steps gets reduced.

2. n bit binary number is represented by $\log_3 2^n$ bits

3. Number of digits required to symbolize in triplex is $\log_3 2$ times less than required in binary.

4. Due to reduced complexity of interconnects and chip area it is simple and energy efficient.

5. Interconnect and pin-out problems that are encountered by the binary integrated circuits are eliminated.

Therefore, triplex logic needs lesser number of bits, memory and number of chip pins. For example, decimal number 8, in triplex it can be represented as $(22)_3$, where in binary it can be represented as $(1000)_2$

III.   CNTFET AND ITS SUITABILITY FOR MVL

The structure of a CNTFET is as same as conventional MOSFET in which semiconducting channel layer is built with semiconducting CNT single layer. The suitability of CNTFET for the application in multi-valued logic lies in the fact that the threshold voltage of the CNTFET can be modified slightly and controlled by proper selection of the chiral vector of the CNT. This is due to the threshold voltage for a CNTFET depends on the band gap of the CNT, Band gap of CNT depends on the orientation of the graphene sheet to obtain the CNT. If (n, m) denotes the chiral vector, which be influenced by on the direction of rolling of the graphene sheet, of the CNT which is used in the channel region of the CNTFET then the diameter of the CNT is given as:

$$dCNT = a/r\pi(n2+m2+nm)1/2$$

where r|a1|=|a2|=1.42*square root of 3=2.46 amstrong
Here a1   and a2 are the primitive lattice vectors of graphene from which the CNT is obtained
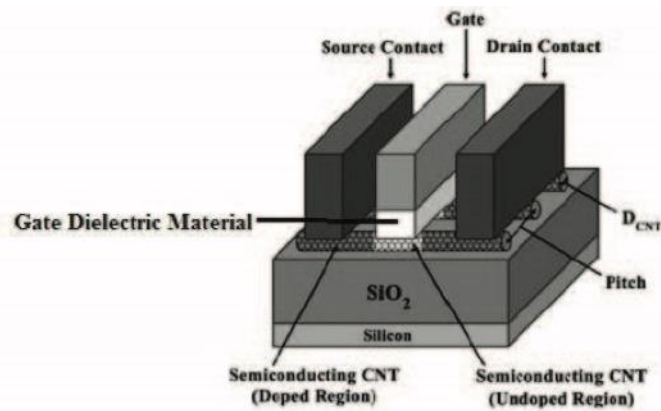
Fig: 1 Structure of CNTFET

As shown in Fig.1, channel region is created by placing undoped CNT under the gate and heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON- state. While the gate potential increased, the device is electro statically turned on or off via the gate and the threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half band gap that is an inverse function of the diameter and is given as:

$$V_{th} = \frac{aV_u}{43ed_{CNT}}$$

Here V_u = 3.033 eV is the carbon $\pi - \pi$ bond energy in the tight binding model, e is known as the unit electron charge, d_{CNT} is the diameter of the CNT plotted in the channel. By this we know clearly that the threshold voltage of a CNTFET varies inversely with the diameter of the CNT and it can be modified to a required value by choosing proper chiral vector. For this major advantage of CNTFET to be used for triplex logic.

IV.   TRIPLEX LOGIC GATES AND HALF   ADDER

Basics of triplex logic and its representation in terms of voltage level is discussed in this section. And the best recent reported half adder circuits from literature are used. Based on this circuit, improved two half adder circuits are offered in next section.

In triplex logic three symbols used are 0, 1 and 2. The voltage level used in terms of Vdd to represent each symbol is given in Table 1. Using this triplex logic

various logic gates   like inverter, NAND, NOR, AND, OR are reported in literature [5].

TABLE 1: LOGIC SYMBOL AND VOLTAGE LEVEL USED IN TRIPLEX LOGIC

Logic Value	Voltage Level
0	0
1	(1/2)Vdd
2	Vdd

In triplex system consist of three types of inverters: negative triplex inverter (NTI), standard triplex inverter (STI) and positive triplex inverter (PTI) [5]. Three inverters symbols and truth tables are given below in Fig. 2 and Table-II.

(a) (b) (c)
Fig 2: Symbols of (a) NTI (b) STI and (c) PTI

Input	Output for STI	Output for PTI	Output for NTI
0	2	2	2
1	1	2	0
2	0	0	0

TABLE 2: TRUTH TABLE FOR STI, PTI AND NTI

For understanding other logic gates, we will assume X_i, X_j are two inputs given as X_i, $X_j = \{0, 1, 2\}$. After that the basic logical operations in triplex logic can be understood as follows:
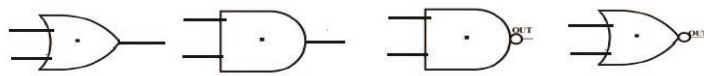
OR : $X_i + X_j = max(X_i, X_j)$

AND : $X_i . X_j = min(X_i, X_j)$

NAND : $\overline{X_i . X_j} = \overline{max(X_i . X_j)}$

NOR : $\overline{X_i + X_j} = \overline{min(X_i + X_j)}$

The various symbols used for these triplex logic gates are shown in Fig. 3.

Fig. 3: Symbols used for triplex logic gates

A triplex decoder consists of a one-input, three-output combinational circuit. It generates unary functions for an input x. The response of the triplex decoder to the input x is given by

$X_k = \{2\ 0\quad if\ x\quad if\ x = k \neq k$

Where both x and k can take any values 0, 1 and 2. Using this type of triplex logic gates, a half adder is designed and shown in Fig. 4 [19]. Table III is the truth table for this triplex adder. An improved version of adder is in our proposed circuit, the AND-OR circuit is replaced by NAND –NOR circuit as shown in Fig 6. due to this the number of transistor is reducing. Again the 3 AND and 1 OR gate combination of Fig. 5 is replaced by transistor level circuit as shown in Fig. 7. This also reduced the number of transistors to 94.
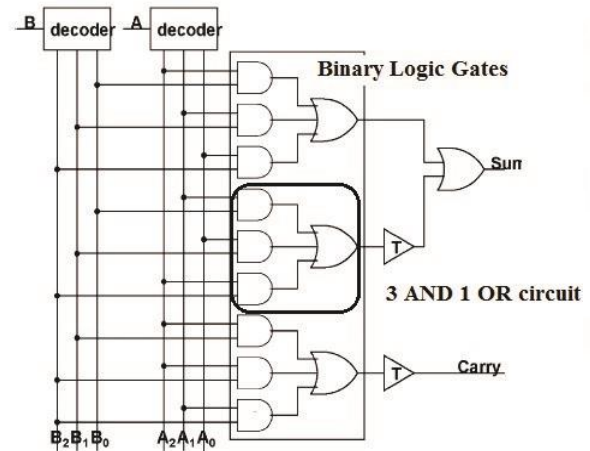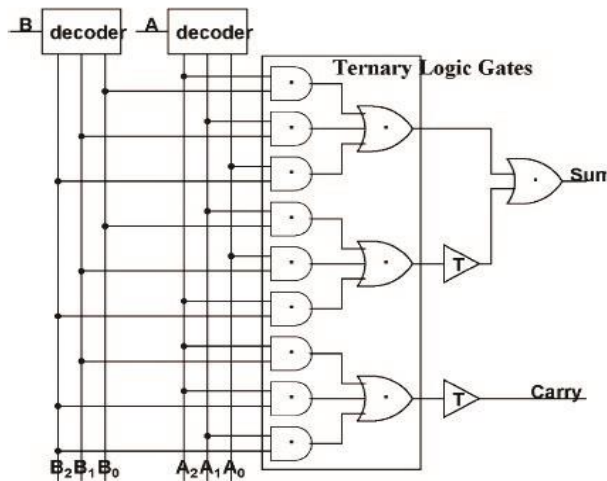
Fig.4 Triplex half adder

Fig 5: Tenary half adder replacing portion of triplex logic by binary logic gates

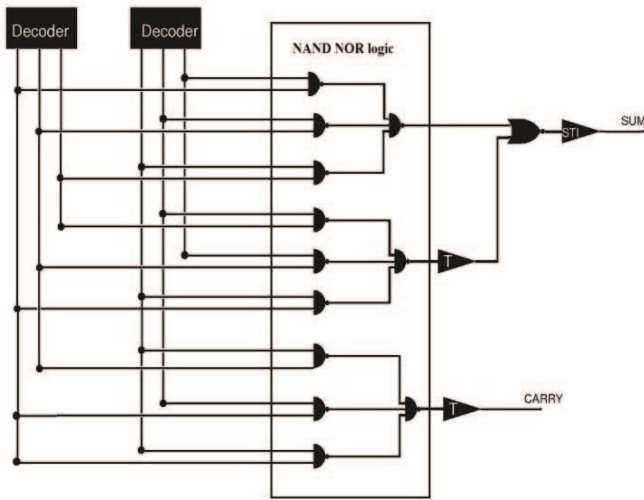| A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

TABLE 3: TRUTH TABLE OF HALF ADDER

Designed and reported by Lin et.al [5]. In this design the triplex logic gates are replaced with binary logic gated as shown in Fig. 5. This replacement of triplex logic gates by binary logic gates has reduced the transistor count and hence improved performance.
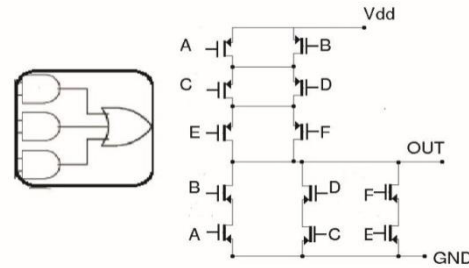
V. PROPOSED TRIPLEX HALF ADDER

The triplex half adder circuit given in Fig 5 uses binary logic gates. This circuit is implemented using AND –OR logic gates.

Fig 6: NAND- NOR implementation of half adder circuit

The two circuits which are proposed are created and the circuits of the references [5] and [19] are

Fig 7: Transistor level implementation of 3 AND 1 OR gate

implemented using HSPICE and simulated. The simulation results are summarized in Table IV. The results of simulation show that the proposed circuit achieves up to 40% delay advantage and 39% power advantage. This advantage is because of the reduced complexity of circuit.

TABLE 8: PERFORMANCE COMPARISONS

Circuit type	No of Tr	Delay Psec	% delay advwrt [19]	Power in μw	% power advwrt [19]	PDP
Ref [19]	158	66.44	-	1.191		79.130
Ref [5]	130	41.425	37	0.84	29	34.797
NAND- NOR	112	39.217	40	0.645	45	25.294
Tr. Level	94	39.74	40	0.718	39	28.533

VI.   CONCLUSION

Two improved circuits for triplex half adder are suggested. All simulations have been performed in HSPICE [20] and Stanford model are used CNTFET. Simulation results have confirmed and the power, delay improvements is possible by the proposed logic. The circuits give 40% delay advantage and up to 39 % power advantage. Thus this half adder can be used by complex arithmetic circuits.

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