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Real Time Signal Quality Aware Internet of Things (IOT) Framework for FPGA Based ECG Telemetry System and **Development of Android Application**

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ABSTRACT

LITSRD

Day by day the scope & use of the electronics concepts in bio-medical field is increasing gradually. A novel approach to the design of real time ECG signal acquisition system for patient monitoring in medical application, FPGA (Field Programmable Gate Array) is the core heart of proposed system which is A typical ECG tracing of normal heartbeat consists of configured and programmed to acquire using ECG (Electrocardiogram) sensor. In this paper a new concept of ECG telemetry system is discussed along with signal quality aware IoT framework for energy efficient ECG monitoring system. Tele monitoring is a medical practice that involves monitoring patients who are not at the same location as the healthcare provider. The purpose of the present study is use to identify heart condition and give the information to the doctor. The objective of the study is to improve the doctor-patient ratio and evaluation of cardiac diseases in the rural population. The proposed system electrocardiogram (ECG) monitoring for the controlled by FPGA and implemented in the form of android application. ...

Keyword- FPGA (Field programmable gate array), Electrocardiogram (ECG) signals, IoT (Internet of Things)

I. **INTRODUCTION**

The word electrocardiography is evolved from Greek word Kardia which means Heart. ECG that is electrocardiography is a process of interpretation of heart activity over the period of time and is detected by electrodes attached to the surface of body. An ECG is used to measure the heart's electrical conduction system. It picks up electrical impulses generated by the polarization and depolarization of cardiac tissue and translates into a waveform. The waveform is then used to measure the rate and regularity of heartbeats,

as well as the size and position of the chambers, the presence of any damage to the heart, and the effects of the drugs or devices used to regulate the heart, such as a pacemaker.

a P wave, a QRS complex and a T wave. Data acquisition products server as a focal point in a system, tying together a wide variety of products such as sensor that indicate temperature, flow, levels, pulse rate, electrocardiograph etc.

The core heart of the proposed system is field programmable gate array (FPGA) which is configured and programmed to acquire a real time data. Real time data from the process is acquired using ECG sensor. Signal conditioners are designed for each sensor. Signal conditioners are interfaced with FPGA through ADC and MAX 232 for PC interfacing. Output of the system is displayed waveform on PC.

An electrocardiogram is a test that checks for problem with the electrical activity of our heart. An ECG translates the heart's electrical activity into line tracing on paper. The spikes and dips in the line tracing are called waves. The ECG signal consist of P,

- Q, R, S, T waves. The function of each wave is-
- P Wave- represents the atrial contraction
- > QRS ventricular complex represents the contraction.
- R peaks- represents a heartbeat. \geq
- T wave- represent the last common wave in an \geq ECG. The electrical signal is produced when the ventricles are repolarizing.



Fig. 1- ECG signal Characteristics

II. RELATED WOEK

Several implementations of finding response time of Real-Time System exist. Also there are several implementations of performance analysis of IoT based Health Care Monitoring for Real-Time System. Also there are novel implementations of Signal Quality Aware ECG Telemetry System for continuous cardiac health monitoring applications. A brief survey's mentioned as below-

Udit Satija, [2016] proposes a novel signal quality aware IoT-enabled ECG telemetry system for continuous cardiac health monitoring applications. The main purpose of these system is design and development of light weight ECG signal quality assessment method for automatically classifying the acquired ECG signal into acceptable or unacceptable class and real time implementation of proposed IoT enabled ECG monitoring framework.[1]

R.Harini1, [2015] ECG is identify heart condition in the rural underserved population where the doctor patient ratio is low and access to health care is difficult. The purpose of these system was clinical validation of handheld ECG as a screening tool for evolution of cardiac diseases in the rural population. [9]

B. Khaleelu Rehman1, [2017] The methodology of ECG FIR filter based on FPGA. The ECG signal is processed and implemented on FPGA platform. The filtered signal is subject to short time Fourier Transform by medical experts. A implication can be made by medical experts. A recorded ECG signal is used as test input and to test the implemented modules on FPGA. [5]

Sande Seema, [2010] propsed the de-noising of ECG signal also design algorithm for IIR and FIR filter in

MATLAB environment to de-noise ECG signal and test the designed algorithm on modelsim these signal transfer digital filter algorithm on FPGA plateform and to analyze the complexity and accuracy of digital filter on MATLAB.[15]

P. Girish, B .V .Ramana, [2014] A real time ECG monitoring system featuring HEV analysis and wireless data transmission through radio frequency based on a SoC development platform. In this system modelsim Xillinx Edition and Xillinx ISE will be used simulation and synthesis respectively. The Xilinx chip-scope tool will be used to test the FPGA inside result while the logic running on FPGA. [11]

Yongming Yang, [2007] A real time ECG monitoring system is proposed based on FPGA. The FPGA chip is taken as the centrol microprocessor and applies structured design on VHDL to collect and transmit real-time ECG signals. It contain low power consumption to carry around and long usage time. The digital filtering and data compression arithmetic are also integrated in the FPGA chip and can be improved or added with some other modules with software modification. It is more intelligent compared with existing portable ECG monitoring system. [20]

III. BLOCK DIAGRAM

The system is used to monitor ECG. Data is digitized with an FPGA microcontroller and send to a computer. The system s portable and runs on less power. The system improves the quality of patient monitoring and eliminates the need for nurses to repeatedly manually perform these measurement.



Fig.2- Block diagram of FPGA based ECG patient monitoring system.

A] FPGA-

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing, hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) FPGAs can be used to implement any logical function that an ASIC could perform.

The ability to update the functionality after shipping, partial of the portion of the design and the low nonrecurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications. FPGAs contain programmable logic components called "logic hierarchy blocks", and a of reconfigurable interconnects that allow the blocks to be "wired together" somewhat like many (changeable) logic gates that can be inter-wired in (many) different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. The Spartan-6 family of Field Programmable Gate Array specifically designed to meet the needs of high volume costsensitive consumer electronic.

B] ECG Sensor-

The AD8232 is an integrated signal conditioning block for ECG and other bio potential measurement J Fig. 3 Signal Quality-aware framework applications. It is designed to extract, amplify, and filter small bio potential signals in the presence of The main focus on design noisy conditions, such as those created by motion or remote electrode placement. This design allows for an ultra-low power analog-to-digital converter (ADC) or an embedded microcontroller to acquire the output signal easily.

C] ADC-

An analog-to-digital converter (ADC, A/D, or A-to-D) is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal. An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to digital number а representing the magnitude of the voltage or current. Typically digital the output is a two's complement binary number that is proportional to the input, but there are other possibilities.

D| RS232-

RS 232 is a serial communication cable used in the system. Here, the RS 232 provides the serial communication between the microcontroller and the outside world such as display, PC or Mobile etc. So lit is a media used to communicate between microcontroller and the PC. In our system the RS232 serves the function to transfer the data in between PC and the FPGA, for the further operation of the system

E] COMPUTER /PC-

Computer / PC is used in a project to visualize the output of the application. Computer / PC is interfaced for the Electrocardiography. A waveform of ECG can be visualize on Computer /PC.

IV. **PROPOSED METHODOLOGY** Al For IOT Framework -

The main modules of signal quality-aware (SQA)-IoT framework are illustrated in Fig. It consists of three modules: (i) ECG signal sensing module, (ii) automated signal quality assessment module, and (iii) signal-quality aware ECG analysis and transmission module.



and real-time implementation of automated ECG signal quality assessment method and validation of the effectiveness of the proposed SQA-IoT framework under resting, ambulatory and physical activity conditions, The proposed automated ECG signal quality assessment (ECG-SQA) method consists of three steps such as flat-line (or ECG signal absence) detection, abrupt baseline wander extraction, and high-frequency noise detection and extraction to compute the signal quality index (SQI) for assessing the clinical acceptability of ECG signals. In this work, the ECG-SQA is implemented based on the-based filtering, turning points and decision rules.

I] HF Noise Detection –

The high frequency (HF) noises such as muscle artifacts, power line interference, motion artifacts, pause and instrument noise are introduced in the acquired ECG signal. Apply decision rules for detecting the ECG segment with HF noises-

$$SQI_{HF} = \begin{cases} 1 & R1 \parallel R2 \\ 0 & otherwise \end{cases}$$

where R1 is true if a total number of turning points in any block (tpk) exceeds 5% of the number of samples (P * F s, where, F s is the sampling frequency of the signal) in that block and R2 is true if the distance between two turning points <math>rk is less than two.

If SQIHF = 1 then the segment is classified as a HF noise segment. Otherwise the segment is classified as a high frequency noise-free ECG segment.

II] ECG signal absence detection-

Due to the disconnection of electrodes with skin and the electronic component saturation, sensing device exhibits the absence of ECG signal information in the acquired signal. In practice, observation to the recording shows the presence of zero amplitude flat line (ZFL), only baseline wander (OBW), and the long pause with physiological and external noises. Existing approaches were developed for detection of ZFL event. It is based on turning points (TP) which can be computed as mentioned in Algorithm.

$$SQI_{FL} = \begin{cases} 1 & t_p > 0.65M \\ 0 & otherwise \end{cases}$$

If SQIFL = 1 then the segment is classified as a flat line or ECG signal absence segment. Otherwise the segment is further processed for detecting the presence of high frequency noises.

III] Abrupt Change Detection-

The ECG signals are corrupted by baseline wanders that are mainly caused by respiratory activity, body movements, skin-electrode interface, varying impedance between electrodes and skin due to poor electrode contact.

By using FIR Based –The basic structure of FIR filter is like a sub-section of the delay lines. Each section of the output of the weighted cumulative, the FIR coefficient is-

$$y(nT) = \sum_{k=0}^{n-1} h(k) x(n-k)$$

The baseline wander signal is obtained as $b[n] = x[n] - x \sim [n]$

Where b(n) is the baseline wander signal and $x \sim (n)$ is the baseline wander removed signal which is computed as

$$\tilde{x}(n) = \frac{1}{N} \sum_{n=0}^{N-1} \tilde{X}(k) e^{\frac{jn\pi k}{N}}$$

The detection decision rule is given by-

$$SQI_{ABW} = \begin{cases} 1 & \max\{|\mathbf{d}|\} > \gamma \\ 0 & \text{otherwise} \end{cases}$$

Where SQIABW denotes the signal quality index (SQI) for the presence of abrupt baseline drift (ABW) event. Here, the γ is chosen as 0.2 mV for detecting abrupt baseline wander which can distort the ST segment and other low-frequency components of the ECG signal. The ECG signal with abrupt baseline wander event is classified as an *unacceptable*. The ECG signal with slowly varying baseline wander is classified as an *acceptable* since it can be removed from the signal without significantly distorting the PQRST complexes.

IV] ECG Signal Quality Grading-

The grading of acquired ECG signal based on the decision scores obtained for the detection of abrupt baseline wander, ECG signal absence, and high frequency noises. The ECG signal is graded with three classes such as Good, Intermediate and bad based on the HF noise score. The presence of flat line and abrupt baseline wander may result in noisy clinical features. Based upon assessment results, it is noted that the some morphological features and RR intervals can be measured from the ECG signal with some level of HF noises. Thus, we grade the noisy ECG signal into intermediate and bad. The value of γ H is chosen as 0.1% of the maxima or minima in the HF noise detection stage for detecting severe noise or bad quality signal. While the noise level threshold yH is set to 0.05% of the maxima or minima for grading the noisy signal into intermediate class.

$$\mathrm{SQG} = \begin{cases} \mathrm{Good} & \mathrm{SQI} = 0 \\ \mathrm{Intermediate} & \mathrm{SQI} = 0.5 \\ \mathrm{Bad} & \mathrm{SQI} > 0.5 \end{cases}$$

Where overall signal quality index (SQI) is computed as

$$SQI = SQIABW + SQIFL + SQIHF$$

Good quality indicates the ECG signal with acceptable level of noise which does not distort the morphological features while *intermediate* and *bad* indicate the medium and high level of noise or poor quality, respectively. The intermediate class of ECG signals may be considered for application-specific ECG signal analysis systems.

B] For Androd Application-

- ➤ ALGORITHM-
- 1. Initialize central processing unit
- 2. Initialize Ports
- 3. Initialize memory
- 4. Initialize ADC
- 5. Connect 3-leads of electrode in correct place
- 6. Read the signals from the sensor and transmit signals to the amplifier
- 7. Convert analog signal to digital signal using ADC3204
- 8. Display the ECG signal on PC
- 9. Also display on Android phone

V. SYSTEM IMPIMENTATON

Al Software Implementation

1.1 Mit-Bih Database

The dataset used in this study is obtained from Physiobank entitled MIT-BIH Arrhythmia Database available on-line. MIT-BIH Arrhythmia Database which having sources of ECGs includes set of over 4000 long-term Holter recorders, which was obtain from Beth Israel Hospital Arrhythmia Laboratory. Each signal is recorded with 360 sampling frequency which having 11-bit resolution with 10 mv range. MIT-BIH Arrhythmia Database where annotated ECG signals are described by a text header file (.hea), a binary file (.dat) and a binary annotated file (.atr). Header file consists of detailed information such as number of samples, sampling frequency, format of ECG signal, type and number of ECG leads, patient's history and the detailed clinical information. In binary data signal file, the signal is stored in 212 format which means each sample requires number of lead times 12 bits to be stored and the binary annotation file consists of beat annotation from which half of this database has been freely available .For EMG dataset is obtained from MIT-BIH Noise stress database from PhysioBank. Noise stress database includes 12 halfhour ECG recordings and 3 half-hour recordings. This is having a noise typical in ambulatory ECG recordings. PhysioBank noise recordings were taken by physical activities of volunteers. For ECG recording 3 noise records were assembled. These recordings were contain predominantly baseline wander (as 'bw'), muscle artifact (as 'ma') which also known as EMG noise and third one is electrode motion artifact (as 'em'). From noise stress database records of 'bw' contains primarily baseline wander with low frequency signals, which was caused by motion of the volunteer or the leads. Recorded ECG contains electrode motion artifacts with 'em'

significant amounts of muscle noise and baseline wander. Recorded ECG 'ma' contains primarily muscle noise (EMG) with spectrum, which overlaps that of the ECG, which extends to higher frequency.

1.2 MATLAB

MATLAB is a powerful, comprehensive, and easy to use environment for technical computations, one of its greatest strengths is that MATLAB allows building its own reusable tools. Mat lab is being used for ECG extraction which database stored is at www.physiobank.org. Stored ECG signal can be called in Simulink model from workspace of mat lab. Real time EMG noise is accessed from MIT-BIH noise stress database in the form of .mat file then it is imported into workspace which is added with pure ECG in Simulink model. For designing of FIR low pass filter FDA Tool from MATLAB has been used. Different types of FIR digital filter designed to remove high frequency EMG noise.

1.3 FIR FILTER

FIR filters are widely used because of inherent stability and due to the powerful design algorithms which are exist from them. When FIR filters implement in non-recursive form, linear phase one can obtain with ease. FIR low pass filter is designed by equiripple filtering, least square method, windowing method for designing have been used. In windowing method such as Kaiser, Rectangular, Hamming, Hanning and Blackman functions are designed.





1.5 Simulink model for FIR filter

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Fig4- Simulink Model of ECG De-noising

In above fig-4 it show that the design of FIR filter. The filters are designed using MATLAB FDA Tool by specifying the filter order, cut off frequency and sampling frequency. In the present section, the design considerations of low pass filter, high pass filter, notch filter are elaborated separately for removal of noise signals from ECG using FIR filter. For ECG denoising the digital filter is designed with various orders. Output of this various designs are simulated and analyzed with the help of performance parameters like SNR and MSE.

BJ HARDWARE IMPLEMENTATION CITATIONAL

The implementation of the design is fundamental to move from software to a hardware realization. The implementation technique exploits the parallel structure and the versatility of Field Programmable Gate Arrays (FPGAs) in order to yield a high performance and yet low cost implementation.

The step by step procedures that are used to complete this project are highlighted. They are explained in below. The explanations are important in complete the objectives of the project. As shown in below flow chart, the implementation procedure will be followed. The board at transmitter side will be FPGA board and at the receiver side the board will be Bluetooth model and Arduino in this digital hardware system.



Fig5-Experimental setup of telemetry system



The experimental setup of the system which includes FPGA board, ECG sensor, Arduino& Bluetooth, the ECG waveform display on monitor and Android applicatonis given in below figure:



Fig 6-Experimental setup of system

VI. RESULT AND DISCUSSION || Matlab Simulation Result

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Clean ECG is taken from MIT-BIH which is added with low frequency noise. Simulation was done on SIMULINK available with MATLAB. Fig.7shows pure ECG from MIT-BIH Arrhythmia database of patient shows noisy ECG. Fig.8shows the application of different FIR filter methods on low frequency EMG noise. Equation (1) is used to calculate SNR of filtered signal and mean square error (MSE) from equation (2) is calculated.

 $N \sum (ECG_{raw})^{2}SNR = 10 \log 10^{i=0}$ $N \sum (ECG_{raw} - ECG_{filtered})^{2i} = -----(1)$ $N \sum (ECG_{raw} - ECG_{filtered})^{2}MSE = ^{i=0}$ N = -----(2)



Fig 7- Noisy ECG Signal



Fig 8-Filtered ECG Signal

Types and order of the	ECG Sample	SNR in dB	Mean Square Error (MSE)				
FIR Filter							
Blackman low pass filter (100)	Ecg24	19.21	25.67				
Hamming low pass filter (100)	Ecg24	19.20	25.67				
Hanning low pass filter (100)	Ecg24	19.21	25.67				
Kaiser low pass filter (100)	Ecg24	18.67	25.42				
Rectangular low pass filter (100)	Ecg24	19.11	25.62				

Table 1 - Performances and evaluation of FIR low pass filters on MIT-BIH database. The value shows SNR in dB.

In Table 1 comparison of different FIR method for SNR and MSE is given. Here it can be concluded that FIR method effectively remove the EMG noise without distortion of the ECG signal. In case of Equiripple, Hamming, Hanning order of the filter was increased which increases the complexity of filter designing. So that SNR of FIR filter with Kaiser is (18.67) less than other type of filter. In case of other method the order of the filter easily grow very much .It increases the number of filter coefficient which leads to the large memory requirement and problems in hardware implementation.

B]Hardware Implementation ResultsI]Waveform Analysis-

The output waveforms generated by FIR filter give better filtered output. The output waveforms are generated with normal ECG signal, filtered high pass signal, filtered low pass signal and peak detection as shown in fig.9 below

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Fig.9- De-noising ECG Signal by FIR Filter by using Spartan Hardware kit.

When the real time ECG signal display on the PC then at time it display on the android application. The ECG output waveforms display on the Android phone as shown in fig. 10 -



Fig. 10- ECG waveform display on Android applicaton.

II] DEVICE UTILIZATION SUMMARY AND POWER ANALYSISa) Device Utilization-

After implementation on Spartan FPGA kit, utilization of resources i.e. no of LUTs, Slices, Bonded I/O has been calculated for different types of FIR filter. Fig. 11- shows that Equiripple requires highest no. of slices, flip-flop,4 input LUTs, bonded IOB with 1GCLK. In window method Kaiser has minimum utilization of resources. As it require 87 slices, 156 slices, Flip flop, 111 LUTs, 17 bonded IOB, with 1 GCLK.

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Fig.11- Device Utilization Report of FIR Filter

b) Power analysis-

Power analysis will generate the timing, ISE report and power utilization report for the particular design. Snapshots of Power Analyzer for FIR filter shown in Fig. 12-



Fig.12- Device Utilization Report of FIR Filter

CONCLUSON VII. of Trend in In this research paper, the implementation of FIR filter on FPGA has been introduced. It has been investigated that, the improvement of noisy ECG signals can be achieved by combination of FIR filters. In order to measure the performance of de-noising, SNR of processed ECG is calculated and MSE was determined to find the degree of mismatch between noisy ECG and filtered. The designed FIR filter with Kaiser Window works excellent in removing High frequency interference from noisy ECG conditions utilizing low order of filter. Utilization of resources using FIR filter has been minimizedi. e. less power consumption (74mw)and minted the quality of ECG signal.

This method is more applicable in various applications of ECG monitoring. Use of optimization technique using FPGA platform will improve the quality and processing time. FPGA are finding wide acceptance in medical system. For their ability for rapid prototyping of a concept that requires hardware/software co-design, for performing custom processing in parallel at high data rates.

VIII. FUTURE SCOPE

The implementation of FIR High Pass filter techniques gives better results on higher end FPGA devices like Virtex, which are having more resources and facilities than Spartan devices. This method can be successfully applied with the cascading of IIR and FIR filters for real time ECG systems. Finally, it is seen that an optimum combination can be implemented using FPGA technique.

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