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Review on FPGA Implementation of 16*16 Vedic Multiplier in VHDL Environment

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ABSTRACT

Multipliers are the main key components of many high performance systems such as FIR filters, Microprocessors, Digital Signal Processors, ALU and etc.It improves the speed of the many processors. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras .A high speed complex 16 *16 multiplier design by using urdhvatiryakbhyam sutra is used here, By using this sutra the partial products and sums are generated in one step which there by reduces the design of architecture in processors. It can be used in the applications such as convolution, Fast Fourier Transform (FFT) and in microprocessors. The propagation delay of the processors can be reduced by using this technology.

Keywords: *FIR filters, ALU, Fast Fourier Transform, urdhvatriyakbhyam sutra, Digital Signal Processors*

I. Introduction

The improvement in the VLSI and FPGA technology has brought out advancement in the design of multipliers. Multipliers are more important and the key component in any processor system . the speed performance of the processor depends on the multiplier within the system Vedic multiplier plays an important role in designing of the multiplier . The term 'Veda' means storehouse of knowledge. Vedic Mathematics is an ancient form of mathematics reconstructed from ancient scriptures referred to as Veda .The Vedic multiplication technique is based on 16 Vedic sutras , which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The mathematical operations using, Vedic Method are very fast ,easy and requires less hardware, this can be used to improve the computational speed and efficiency of processors. This paper describes the design and implementation of FPGA for 16*16 Vedic multiplier based on Urdhva Tiryakbhyam sutra (Vertically and Crosswise technique) of Vedic Mathematics. Urdhva Triyabhyam is a type of algorithm used for designing the multiplier they can be used for smaller multiplier operations.

II. TOOLS USED

DEVELOPMENT BOARD:

The Basys 2 FPGA development board is a circuit design and implementation platform for beginners to gain experience building real digital circuits. Built around a Xilinx® Spartan®-3E FPGA and an Atmel® AT90USB2 USB controller, the Basys 2 development board provides complete, ready-to-use hardware suitable for hosting circuits ranging from basic logic devices to complex controllers. A large collection of on-board I/O devices and all required FPGA support circuits are included, so countless designs can be created without the need for any other components.

Four standard expansion connectors allow designs to grow beyond the Basys 2 board using breadboards, user-designed circuit boards, or Pmods (Pmods are

inexpensive analog and digital I/O modules that offer A/D & D/A conversion, motor drivers, sensor inputs, and many other features). Signals on the 6-pin connectors are protected against ESD damage and short-circuits, ensuring a long operating life in any environment. The Basys 2 board works seamlessly with all versions of the Xilinx ISE® tools, including the free WebPACK™. It ships with a USB cable that provides power and a programming interface, so no other power supplies or programming cables are required.

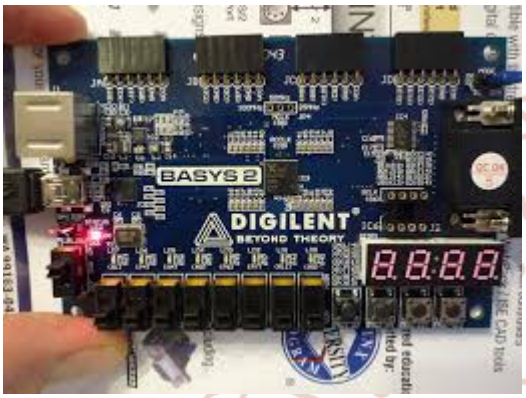

Fig.1 Basy 2 development board

Features:

- User-settable oscillator frequency (25, 50, and 100 MHz), plus socket for a second oscillator
- Three on-board voltage regulators (1.2V, 2.5V, and 3.3V) that allow use of 3.5V-5.5V external supplies
- 4-digit seven-segment display
- USB2 full-speed port for FPGA configuration and data transfers (using Adept 2.0 software available as a free download)
- Four 6-pin headers for user I/Os, and attaching Diligent Pmod accessory circuit boards

SPARTAN 3E FAMILY:

Field Programmable Gate Arrays. Xilinx Inc. The Spartan®-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications

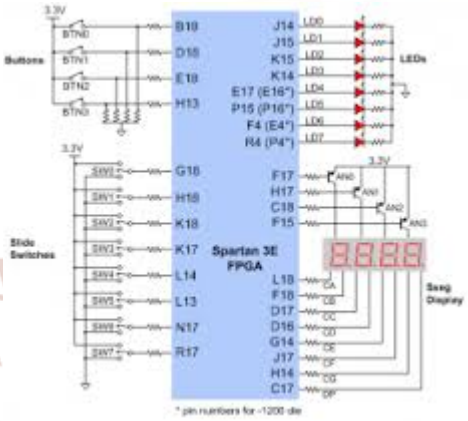

Fig .2 pin description of Spartan 3E

III. DESIGN OF 16*16 VEDIC MULTIPLIER

VEDIC MULTIPLER: (urdhvatriyakbhyam method)

It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

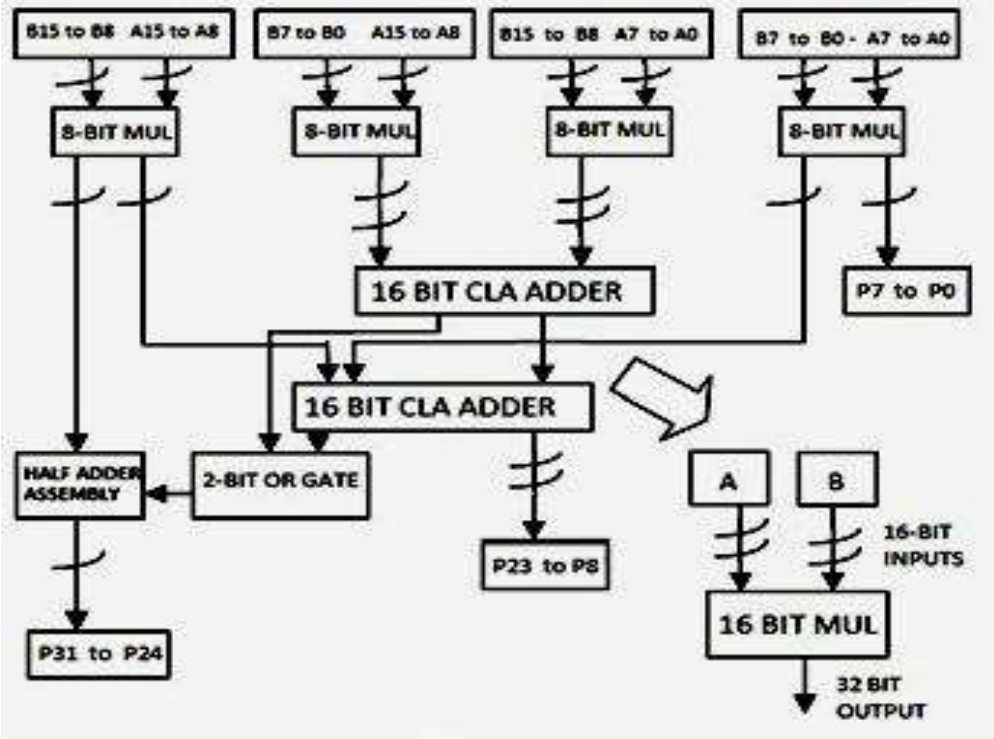

Fig.3 Block of 16*16 vedic multiplier

IV. CONCLUSION

We have designed 16-bit Vedic multiplier using Xilinx 14.4 successfully. The lower bit Vedic multiplier (for Ex. 2-bit, 4-bit, 8-bit) was verified in the standard verification environment of FPGA and are ready to be used. This design is suitable for the applications that require low power consumption and small occupied Si space. The main advantage is they can be implemented in whichever FPGA which reflects they are not dependent on the implementation platform.

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