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Improving Analog Performance and Suppression of Subthreshold Swing using Hetero-Junction Less Double Gate Tunnel FETs

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ABSTRACT

In this paper, we investigated a new device, Hetero-junction less (H-JL) Double Gate Tunnel Field Effect Transistors (DGTFET) with high-k. III-V semiconductor material (like InAs-Si) gives excellent performance when InAs uses at source side, because of low band gap of 0.36 eV it reduces the potential barrier height of source channel interface causing maximum carriers are fastly tunnel across the source to drain in ON state whereas Si, at the drain side as higher bandgap

Of increasing the barrier height of drain channel interface causing lower quantum tunneling occur, as a result good ION/IOFF ratio. The InAs-source JLDGTFET with high-k (Hfo2) at 20 nm channel length provide a tremendous characteristics with high ratio , a point subthreshold swing (SS) and average SS is at room temperature. The simulation study of proposed device is done using sentaurus tools.

Keywords: *Band to Band Tunneling (BTBT), high dielectric material, junctionless, quantum tunnelling, SS, tunnel field effect transistors (TFETs)*

I. INTRODUCTION

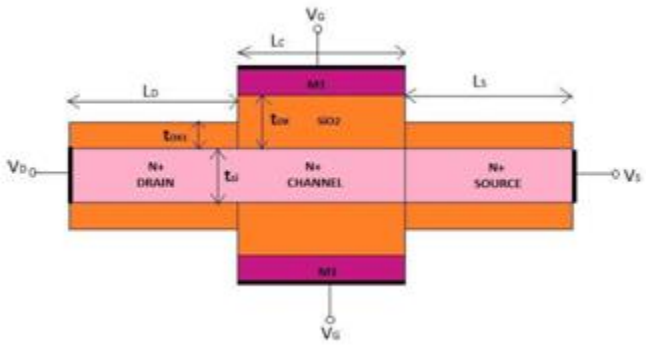
Over the past few decades, the smaller we make a MOSFET, its leaks more current when it was in OFF state because the geometry of device . Beyond 0.5 V, the scaling of MOSFET creating a problem due to their fixed ON state current and subthreshold swing (SS), which is calculated by .

Where T is the temperature, q is the charge, k is the Boltzmann's constant, is transition or depletion region capacitance and is oxide capacitance. At the room temperature, the ideal value of SS is which is nearly to limit of the MOSFET. The quantum tunneling used implies that the TFETs would use much lower energy than that by usual MOSFET during operation, but the I_{ON} current is low in TFETs. For better gate control over the channel and boosting the drive current several multi-gate device structures like Double gate TFETs, Gate all around TFETs etc. has been proposed in last few years. Later on single material gate hetero-dielectric has been proposed to reduce the ambipolar device but it offers high subthreshold swing. In order to reduce the SS of the device dual material device was proposed with an advantage of low SS and ambipolar current but the tunneling current is low. Due to low tunneling probability, we get a low ON drive current in the past devices. For getting a larger ON state drive current and a smaller SS, we have introduced a device structure referred as InAs-source junctionless (JL) double gate tunnel field effect transistors (DGTFETs) with high-k. We have used Indium Arsenide (InAs) for source region to minimize the energy barrier width at the source junction. Whereas, drain material (Si) is kept same, which create high-energy barrier width (because of high band gap energy in comparison to InAs at the drain side in the OFF state to keep the OFF current low. Junctionless device also contribute for ease of fabrication since there is no doping concentration declinations for distinct regions. In this paper, we extracted the parameter like ratio, Drain Transconductance, Input and Output transfer

characteristics of InAs-source JLDGTFETs, SS and also provide a comparative study of proposed device with Ge-source JLDGTFETs and conventional JLTFETs. Section-II provides the device structure and parameters. Section-III deals with the results and discussion. Section-IV deals with references.

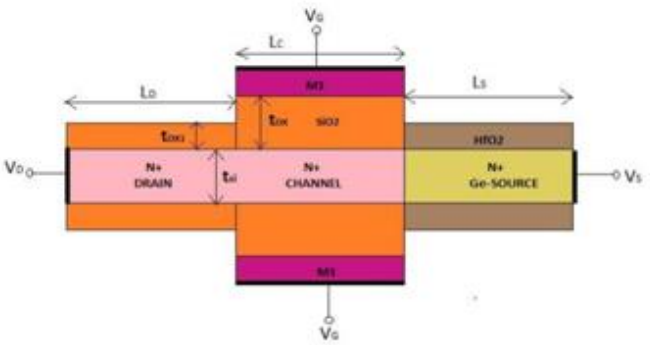
II. DEVICE STRUCTURE AND OPERATION

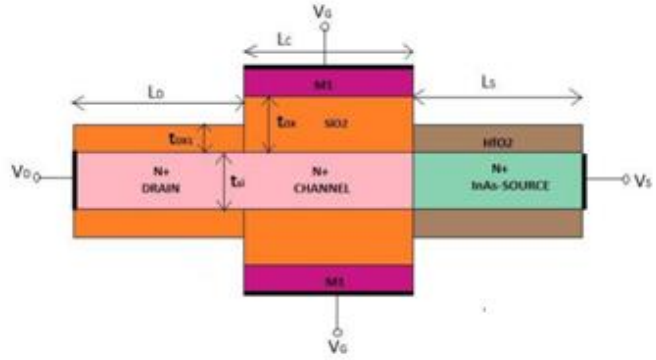
Tunnel FETs is a type diode which is work in reverse biased condition on applying a suitable voltage at drain electrode. When applying a considerable voltage on gate terminal, devices switches on and tunneling starts from source to drain. Fig. 1(a), (b), (c) shows the device cross-sectional view of conventional, Ge-source, and InAs-source junctionless DGTFETs. In these, channel are highly doped with uniform n-type region (concentration = 10^{19} atoms/cm3) silicon thin film is considered for devices. Due to differences in work function (~0.5eV) of channel and gate electrode, a region was created. In OFF state, because of depletion of carriers there is zero current in the device but when the gate voltage greater than flat band voltage, device work in ON state with zero resistance.



(a)

(b)





(c)

Fig 1: Schematic for (a) conventional junctionless double gate TFET (JLDGTFETs), (b) Ge-source junctionless double gate TFETs (GeS-JLDGTFETs) and (c) proposed InAs-source junctionless double gate TFETs (InAsS-JLDGTFETs).

The polysilicon is used to form the gate electrode, which has work function the simulations parameters of the proposed device are:
thickness of silicon film is 10nm, gate oxide thickness 2nm, oxide thickness above the source and drain region is 1 nm, channel length 20nm, source and drain region length is kept 30nm.
All the 2-D simulation method carried out using Sentaurus tools TCAD. The recombination tunnelling generation rate is calculated by nonlocal band-to-band tunneling model. We also activated drift diffusion model, hurkx trap assisted unneling model for simulation. In Shockley read hall model, we used scharfetter parameter from. In proposed device the heterointerfaces increases tunnelling in device and hence results in higher ratio, lower SS and good , which shows the amplification capability of the device is better than the ge-source JLDGTFETs and conventional JLTFETs.

III. RESULTS AND DISCUSSION

Fig 2: Shows the energy band diagram of proposed device in the ON state and in OFF state below the 1nm of silicon and SiO_2 interface of the proposed device. In ON state, the channel of conduction band aligned with the source of valence band due to this the tunneling width decreases hence maximum numbers of carriers are starts tunneling from source to drain means probability of tunneling increased. It also observes that the increment in probability of quantum tunneling due to this the ON current is increases.

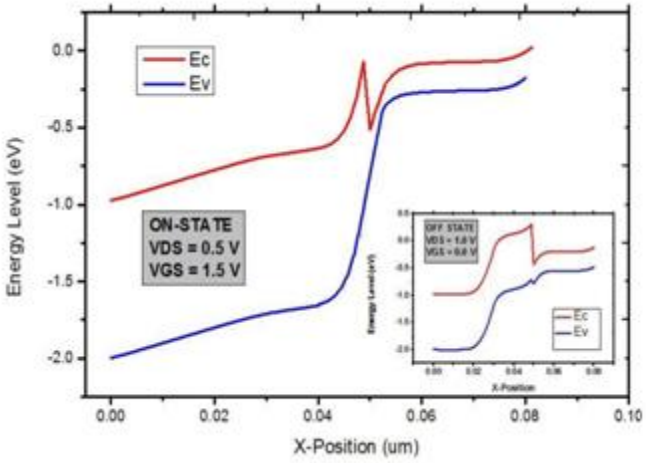


Fig 2: ON state band diagram of proposed device with. Inset: OFF state band diagram of proposed device with

The characteristics comparison of conventional JLDGTFET, Ge-source JLDGTFET and InAs-source JLDGTFETs is shown in Fig. 3. It is clear that I_{ON} (ON current) for the proposed device isit is almost 10 times larger than the ON current of Ge-source JLDGTFETs and 30 times larger than the ON current of conventional JLDGTFETs. In the case of OFF current, for the proposed device I_{OFF} is. Therefore, the ratio is approx, so the switching speed of proposed device is very high. SS is the minimum requirements of gate voltage to increase the drain current by 10 times or one decade. For the proposed device, point sub threshold swing is and the average subthreshold swing is evaluated from the simulated transfer characteristic of InAs-source JLDGTFETs devices.

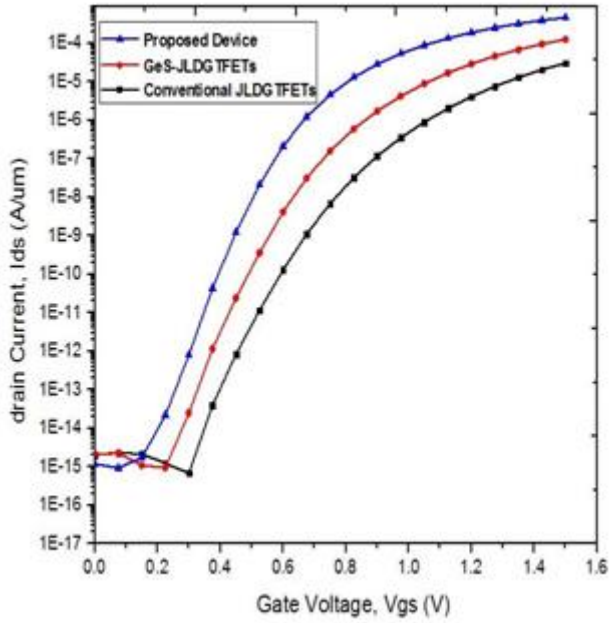


Fig 3: Comparison of characteristics of simulated proposed device with ge-source JLDGTFETs and conventional JLDGTFETs

The output characteristics of proposed device shown in fig. 3, the drain current increases with the increase in drain voltage and at last it was enter in the saturation region. In addition of this, the proposed device demonstrated large value of drain current at minimum value of gate voltage and hence excellent performance than that of Ge-source JLDGTFETs and conventional JLTFET.

In the fig. 4 shows that drain output conductance, G_d = ___ vs. drain to source voltage, V_{DS} for V_{GS} = 1V. This shows the large variation in drain current and gate control over the channel by increasing the gate voltages. The drain current increasing by band-to-band tunnelling mechanism, at high V_{GS} and low V_{DS}, a small increment in V_{DS} causes more carriers transports from the source valence band to channel conduction band through the tunnelling mechanism.

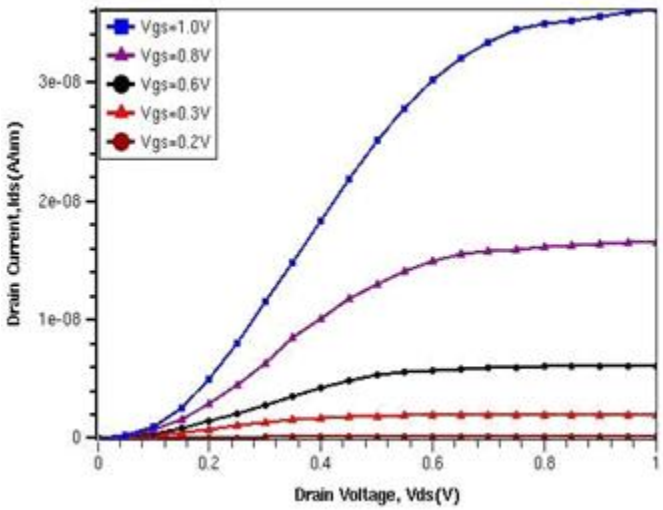


Fig 3: Output characteristics of proposed device with gate voltage variation

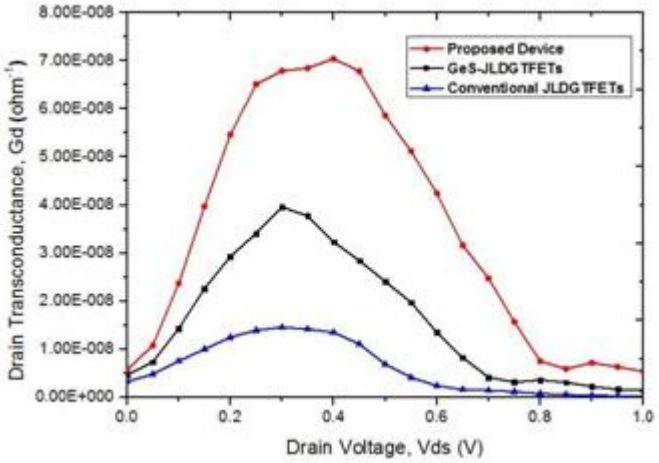


Fig 4: Transconductance vs V_{DS} at V_{GS} = 1V for proposed device, Ge-source JLDGTFETs and conventional JLDGTFETs

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