



## Grid-Connected PV-Wind System with Implementation

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### ABSTRACT

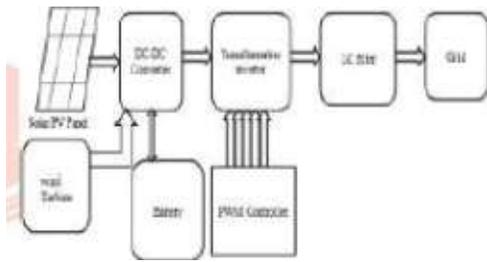
Renewable energy sources are getting more and more widespread, mainly due to the fact that they generate energy by keeping the environment clean. Most of these systems have an isolation transformer included, which if excluded from the system would increase the efficiency and decrease the size of PV installations, furthermore it would lead to a lower cost for the whole investment. For safety reasons grid connected PV systems include galvanic isolation. In case of transformer less inverters, the leakage ground current through the parasitic capacitance of the PV panels, can reach very high values. A common-mode model based on analytical approach is introduced, used to predict the common-mode behavior, at frequencies lower than 50 kHz, of the selected topologies and to explain the influence of system imbalance on the leakage current. It will be demonstrated that the neutral inductance has a crucial influence on the leakage current. Finally simulation results will be shown for the NPC multilevel inverter topology, emphasizing the low leakage current for the case of a grid connection without galvanic isolation.

**Keywords:** *Leakage current, parasitic capacitance, switching converter, NPC*

### 1. INTRODUCTION

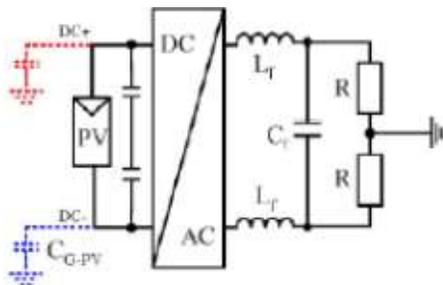
In order to ensure the safety, leakage currents must be the smaller the better in grid connected PV systems. Using the transformers can make the galvanic

connection between the grid and the PV array eliminated. But the transformer is large, heavy, and expensive. Thus, finding a way of high efficiency, low price, light weight, small volume is necessary. The transformer less inverter with low leakage currents can solve the problem in grid connected PV systems, particularly in low-power single-phase systems. So various transformer less inverter topologies have been proposed to meet the point of reducing leakage currents by experts around the world. The full bridge circuit high frequency common-mode equivalent model, and pointed out the way to eliminate leakage currents is the freewheeling voltage is half of the input voltage. Based on the conclusion, the leakage currents of the topologies can be diminished in the following aspects: a) Creating a freewheeling current path, b) Neutral point clamped. In fact, the freewheeling current directions are reversed in different half period of the utility grid. This paper proposes a novel structure based on the idea which is able to create a path can only flow the positive freewheeling current in the positive half period figure 1, and flow the negative freewheeling current in the negative half period respectively, so that it achieve the point of the freewheeling currents directions separation by the IGBTs and diodes. This paper will first introduce the leakage path for transformer less PV systems. Then the comparative analysis on the proposed topology and Heric topology is described. Finally, the simulation results are presented to prove the well performance of the proposed topology in leakage currents.



## II. TRANSFORMER LESS TOPOLOGY ANALYSIS

As discussed in previous works, the common-mode voltage generated by a topology and modulation strategy can greatly influence the ground leakage current that flows through the parasitic capacitance of the PV array. Generally, the utility grid does not influence the common-mode behavior of the system, so it can be concluded that the generated common mode voltage of a certain inverter topology and modulation strategy can be shown using a simple resistor as load. Therefore, in the case of simulations, only a resistive load is used, and the common-mode voltage is measured between the dc+ terminal of the dc source and the grounded middle point of the resistor as shown in Fig. 2.



**Figure 2: Test setup used for common-mode voltage measurement**

In the following, simulation results obtained using MATLAB/SIMULINK are shown. The simulation step size is  $0.1 \mu\text{s}$ , with an 8-kHz switching frequency. Simulation parameters:

$L_f = 1.8 \text{ mH}$  filter inductance;

$C_f = 2 \mu\text{F}$  filter capacitance;

$R = 7.5 \Omega$  load resistance;

$V_{dc} = 350 \text{ V}$  input dc voltage;

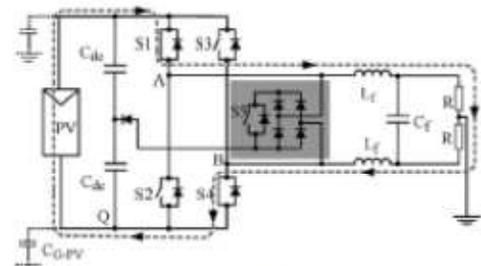
$C_{dc} = 250 \mu\text{F}$  dc-link capacitance;

$C_{G-PV} = 100 \text{ nF}$  parasitic capacitance of PV array;

$F_{sw} = 8 \text{ kHz}$  switching frequency for all cases except that the switching frequency for unipolar Pulse width modulation (PWM) has been chosen to be  $F_{sw} = 4 \text{ kHz}$ , so the output voltage of the inverter has the same frequency for all cases.

## 2.1 HB-ZVR Topology

Another solution for generating the zero-voltage state can be done using a bidirectional switch made of one IGBT and one Diode Bridge. The topology is detailed in Fig. 3, showing the bidirectional switch as an auxiliary component with a gray background. This bidirectional switch is clamped to the midpoint of the dc-link capacitors in order to fix the potential of the PV array also during the zero-voltage vector when S1–S4 and S2–S3 are open. An extra diode is used to protect from short-circuiting the lower dc-link capacitor. During the positive half-wave, S1 and S4 are used to generate the active state, supplying a positive voltage to the load, as shown in Fig. 3. The zero-voltage state is achieved by turning on S5 when S1 and S4 are turned off, as shown in Fig. 4. The gate signal for S5 will be the complementary gate signal of S1 and S4, with a small dead time to avoid short-circuiting the input capacitor. By using S5, it is possible for the grid current to flow in both directions; this way, the inverter can also feed reactive power to the grid, if necessary.



**Figure 3. Active vector applied to load, using S1 and S4 during positive half-wave.**

During the negative half-wave of the load voltage, S2 and S3 are used to generate the active vector and S5 is controlled using the complementary signal of S2 and S3 and generates the zero voltage state, by short-circuiting the outputs of the inverter and clamping them to the midpoint of the dc-link. During the dead time, between the active state and the zero state, there is a short period when the freewheeling current finds its path through the anti parallel diodes to the input capacitor while all the switches are turned off. This is shown in Fig. 5 and leads to higher losses, compared to the HERIC topology, where the freewheeling current finds its path through the bidirectional switch, either through S5 or S6, depending on the sign of the current.

## CONCLUSION

Transformer less inverters offers a better efficiency, compared to those inverters that have a galvanic isolation. On the other hand, in case the transformer is

omitted, the generated common-mode behavior of the inverter topology greatly influences the ground leakage current through the parasitic capacitance of the PV. Bipolar PWM generates a constant common-mode voltage, but the efficiency of the converter is low, due to the two level output voltage. By using unipolar PWM modulation, the output of the converter will have three levels, but in this case, the generated common-mode voltage will have high-frequency components, which will lead to very high ground leakage currents. This paper has introduced a transformer less topology and given an alternative solution for the bidirectional switch, used to generate the zero-voltage state. A NPCMLI is used to provide reduced harmonic voltage to the grid to reduce the harmonics at load current.

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